AXPM11584

3A, 1.5MHz, 28V Buck Converter

Datasheet — May 2020

Description

AXPM11584 is a buck switching regulator with an integrated high-side power mosfet. It provides 3A output with current mode control for fast loop response and easy compensation. The wide 4.5V to 28V input range accommodates a variety of step-down applications, including those in an automotive input environment. A 100μA operational quiescent current allows use in battery-powered applications. High power conversion efficiency over a wide load range is achieved by scaling down the switching frequency at light load condition. The frequency foldback helps prevent inductor current runaway during start-up and thermal shutdown provides reliable, fault tolerant operation. By switching at 1.5MHz, AXPM11584 can minimize EMI (Electromagnetic Interference) related problems. AXPM11584 is available in thermally enhanced SOIC8E package.

Features

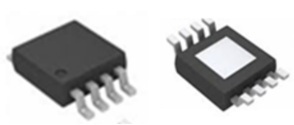
- 4.5V ~ 28V Operating input range
- 100kHz ~ 1.5MHz programmable switching frequency
- High efficiency pulse skipping mode for light load
- Internal soft start
- Internally set current limit without a current sensing resistor

Applications

- High voltage power conversion
- Automotive systems
- Industrial power systems
- Distributed power systems
- Battery powered systems

Table 1 Device Summary

Order code	Package	Packing
AXPM11584	SOIC8E	Tube



SOIC8E

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Figure 1 Block Diagram

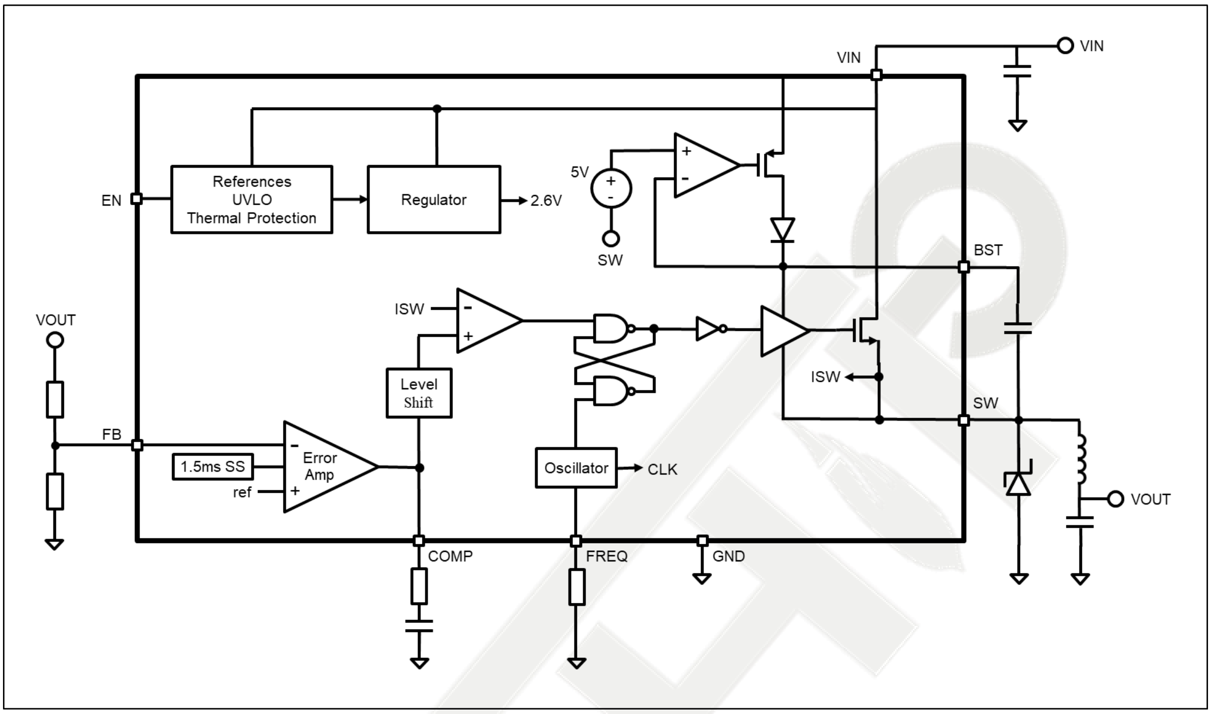
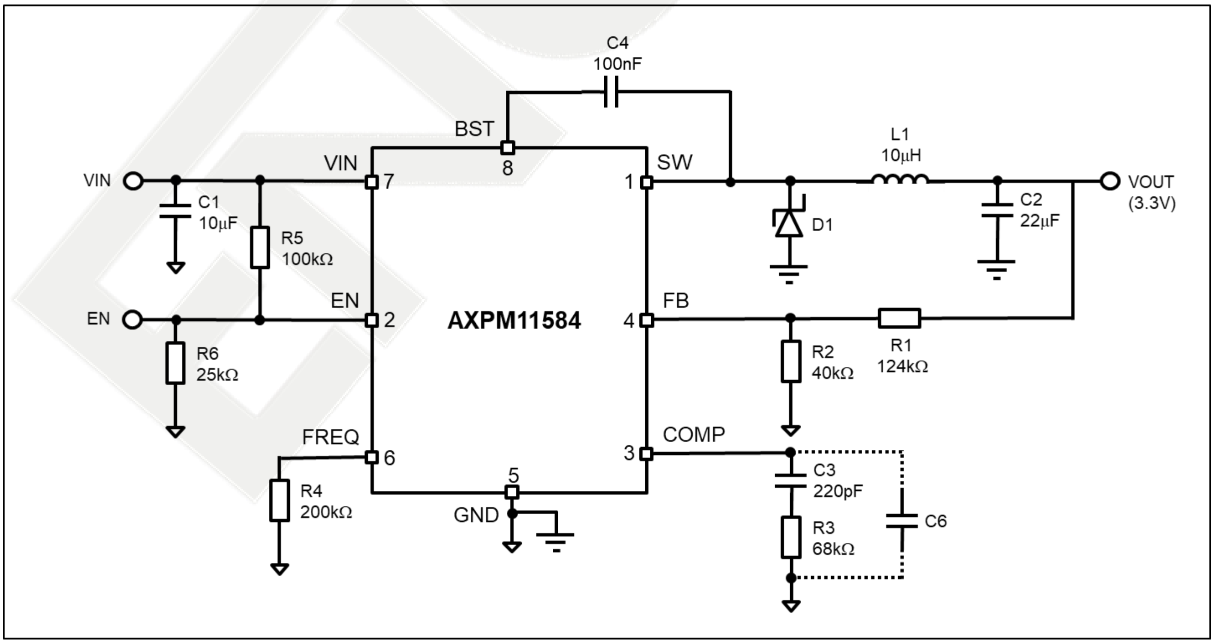


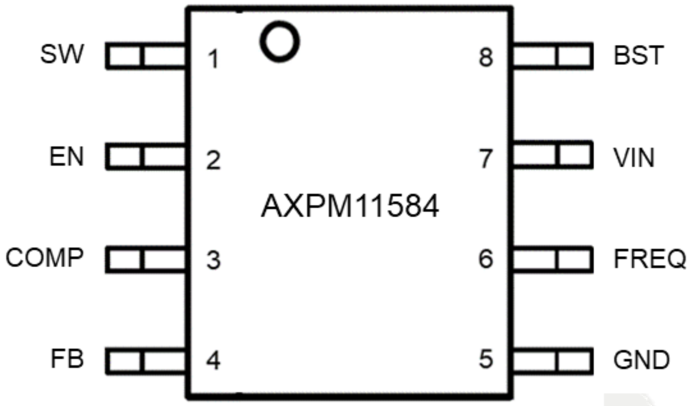
Figure 2 Application Circuit (typical)



2 Pin Description

2.1 Pin Names

Figure 3 Pin Connection



2.2 Pin Functions

Table 2 Pin Functions

Pin number	Pin name	Description
1	SW	Switch Node. This is the output from the high side switch. A low forward drop Schottky diode to ground is required. The diode must be close to the SW pin to reduce switching spikes.
2	EN	Enable Input. Pulling this pin below the specified threshold shuts the device down. Pulling it up above the specified threshold or leaving it floating enables the device.
3	COMP	Compensation. This node is the output of the error amplifier. Control loop frequency compensation is applied to this pin.
4	FB	Feedback. This is the input to the error amplifier. The output voltage is set by a resistive divider connected between the output and GND which scales down VOUT to equal to the internal reference.
5	GND	Exposed Pad Ground. It should be connected as close as possible to the output capacitor to shorten the high current switch path. Connect exposed pad to GND plane for optimal thermal performance.
6	FREQ	Switching Frequency Program Input. Connect a resistor from this pin to ground to set the switching frequency.
7	VIN	Input Supply. This supplies power to all the internal control circuitries. A decoupling capacitor to ground must be placed close to this pin to minimize switching spikes.
8	BST	Bootstrap. This is the positive power supply for the internal high side mosfet driver.

3. Electrical Specifications

3.1 Absolute Maximum Ratings

Table 3 Absolute Maximum Ratings

Symbol	Parameter	Value	Unit
VIN	Supply voltage	-0.3 to +30	V
VSW	Switch voltage	-0.3 to VIN+0.3	V
V_{BST-SW}	BST to SW voltage	-0.3 to +6	V
	All Other Pins	-0.3 to +6	A
Ptot	Power dissipation Tamb = +25°C	2.5	W
Tj	Junction temperature	150	°C
Tstg	Storage temperature	-55 to +150	°C

3.2 Thermal Data

Table 4 Thermal Data

Symbol	Parameter	Value	Unit
Rth j-case	Thermal resistance junction-to-case Max.	10	°C/W

3.3 Electrical Characteristics

VIN = 12V; VEN = 2.5V; VCOMP = 1.4V; Tamb = +25°C; unless otherwise specified.

Table 5 Electrical Characteristics

Symbol	Parameter	Test conditions	Min	Typ	Max	Unit
Toper	Operating temperature		-20	-	+85	°C
VIN	Supply voltage		4.5	-	28	V
VOUT	Output voltage		0.8	-	25	V
VFB	Feedback Voltage	4.5V < VIN < 28V	0.776	0.800	0.824	V
Rdson	Upper switch on-resistance	VBST – VSW = 5V		150		mΩ
Ileak	Upper switch leakage	VEN = 0V, VSW = 0V, VIN = 28V.		1		µA
Ilim	Current limit		4.0	4.7		A
Gcs	COMP to current sense transconductance			3		A/V
Gv	Error amp voltage gain			200		V/V
Gea	Error amp transconductance	ICOMP = ±3µA		180		µA/V
Iea-so	Error amp minimum source current	VFB = 0.7V		15		µA
Iea-si	Error amp minimum sink current	VFB = 0.9V		-15		µA
UVLO	VIN UVLO Threshold		2.7	3.0	3.3	V
UVLOhys	VIN UVLO Hysteresis			0.35		V
Tss	Soft start time	0V < VFB < 0.8V		1.5		ms
Fosc	Oscillator frequency	RFREQ = 100kΩ		0.9		MHz
Isd	Shutdown Supply Current	VEN = 0V		6		µA
Iq	Quiescent Supply Current	No load, VFB = 0.9V		90		µA
Tsd	Thermal shutdown			150		°C
Tsd-hys	Thermal shutdown Hysteresis			15		°C
Toff-min	Minimum off time			100		ns
Ton-min	Minimum on time			100		ns
VEN-th	EN up threshold		1.35	1.50	1.65	V
VEN-hys	EN hysteresis			0.3		V

4 Functional Description

4.1 Overview

AXPM11584 is a variable frequency, non-synchronous, buck switching regulator with an integrated high side power mosfet. It provides a highly efficient solution with current mode control for fast loop response and easy compensation. It features a wide input voltage range, internal soft start control and current limiting.

4.2 PWM Control

At moderate to high output current, AXPM11584 operates in a fixed frequency, peak current control mode to regulate the output voltage. A PWM cycle is initiated by the internal clock. The power mosfet is turned on and remains on until its current reaches the value set by the COMP voltage. When the power switch is off, it remains off for at least 100ns before the next cycle starts. If, in one PWM period, the current in the power mosfet does not reach the COMP set current value, the power mosfet remains turn on, saving a turn off operation.

4.3 Error Amplifier

The error amplifier compares the FB pin voltage with the internal reference and outputs a current proportional to the difference between the two. This output current is then used to charge the external compensation network to form the COMP voltage, which is used to control the power mosfet current. During operation, the minimum COMP voltage is clamped at 0.9V and its maximum is clamped at 2V. COMP is internally pulled down to GND in shut down mode. COMP should not be pulled up beyond 2.6V.

4.4 Internal Regulator

Most of the internal circuitries are powered from the internal regulator. This regulator takes the VIN input and operates in full VIN range. When VIN is greater than 3V, the output of the regulator is in full regulation. When VIN is lower than 3V, the output decreases.

4.5 Enable Control

AXPM11584 has a dedicated enable control pin (EN). With high enough input voltage, the device can be enabled and disabled by EN which has positive logic. Its falling threshold is 1.2V, and its rising threshold is 1.5V. When left floating, EN is pulled up to about 3V by an internal 1μA current source so it is enabled. To pull it down, 1μA current capability is needed. When EN is pulled down below 1.2V, the device is put into the lowest shut down current mode. When EN is higher than 0V but lower than its rising threshold, the device is still in shut down mode but the shutdown current increases slightly.

4.6 Under Voltage Lockout (UVLO)

Under voltage lockout (UVLO) is implemented to protect the device from operating at insufficient supply voltage. The UVLO rising threshold is about 3V while its falling threshold is about 2.6V.

4.7 Soft Start

The soft start is implemented to prevent the converter output voltage from overshooting during start up. When the device starts, the internal circuitry generates a soft start (SS) voltage ramping up from 0V to 2.6V. When it is lower than the reference, SS overrides the reference, so the error amplifier uses SS as the reference. When SS is higher than the reference, the reference regains control.

4.8 Thermal Shutdown

Thermal shutdown is implemented to prevent the device from operating at exceedingly high temperatures. When the silicon die temperature is higher than its upper threshold, it shuts down the whole device. When the temperature is lower than its lower threshold, the device is enabled again.

4.9 Bootstrap

The power mosfet driver is powered by an external bootstrap capacitor. The bootstrap capacitor is charged and regulated to about 5V by the dedicated internal bootstrap regulator. When the voltage between the BST and SW node is lower than its regulation, a pass transistor connected from VIN to BST is turned on. The charging current path is from VIN, BST and then to SW. External circuit should provide enough voltage headroom to facilitate the charging. If VIN is sufficiently higher than SW, the bootstrap capacitor can be charged. When the power mosfet is ON, VIN is about equal to SW so the bootstrap capacitor cannot be charged. When the external diode is on, the difference between VIN and SW is largest, thus making it the best period to charge. When there is no current in the inductor, SW equals the output voltage VOUT so the difference between VIN and VOUT can be used to charge the bootstrap capacitor.

At higher duty cycle operation condition, the time period available to the bootstrap charging is less so the bootstrap capacitor may not be sufficiently charged. In case the internal circuit does not have enough voltage and the bootstrap capacitor is not charged, extra external circuitry can be used to ensure the bootstrap voltage is in the normal operational region.

4.10 Current Comparator and Current Limit

The power mosfet current is accurately sensed via a current sense mosfet. It is then fed to the high-speed current comparator for the current mode control purpose. The current comparator takes this sensed current as one of its inputs. When the power mosfet is turned on, the comparator is first blanked till the end of the turn on transition to avoid noise issues. The comparator then compares the power switch current with the COMP voltage. When the sensed current is higher than the COMP voltage, the comparator output is low, turning off the power mosfet. The cycle-by-cycle maximum current of the internal power mosfet is internally limited.

4.11 Start Up and Shut Down

If both VIN and EN are higher than their appropriate thresholds, the device starts. The reference block starts first, generating stable reference voltage and currents, and then the internal regulator is enabled. The regulator provides stable supply for the remaining circuitries.

While the internal supply rail is up, an internal timer holds the power mosfet off for about 50μs to blank out the start-up glitches. When the internal soft start is enabled, it first holds its SS output low to ensure the remaining circuitries are ready and then slowly ramps up. Three events can shut down the device: EN low, VIN low and thermal shutdown. In the shutdown procedure, power mosfet is turned off first to avoid any fault triggering. The COMP voltage and the internal supply rail are then pulled down.

4.12 Programmable Oscillator

AXPM11584's oscillating frequency is set by an external resistor, Rfreq from the FREQ pin to ground. The value of Rfreq can be calculated from:

$$\mathrm{Rfreq} = \frac{180000}{\mathrm{fs}}$$

5 Components Selection

5.1 The Power Setting the Output Voltage

The output voltage is set using a resistive voltage divider from the output voltage to FB pin. It is given as follows:

$$\mathrm{VOUT} = \mathrm{VFB}\ \mathrm{x}\ \frac{\mathrm{R1} + \mathrm{R2}}{\mathrm{R2}}$$

About 20µA current from high side BS circuitry can be seen at the output when AXPM11584 is at no load. In order to absorb this small amount of current, keep R2 under 40kΩ. With this value, R1 can be determined by:

$$\mathrm{R1} = 50 \times (\mathrm{VOUT} - 0.8)$$

5.2 Inductor

The inductor is required to supply constant current to the output load while being driven by the switched input voltage. A larger value inductor will result in less ripple current which will result in lower output ripple voltage. However, the larger value inductor will have a larger physical size, higher series resistance and lower saturation current.

A good rule for determining the inductance to use is to allow the peak-to-peak ripple current in the inductor to be approximately 30% of the maximum switch current limit. Also, make sure that the peak inductor current is below the maximum switch current limit. The inductance value can be calculated by:

$$\mathrm{L1} = \frac{\mathrm{VOUT}}{(\mathrm{fs}\ \mathrm{x}\ \Delta\mathrm{IL})}\ \mathrm{x}\ (1 - \frac{\mathrm{VOUT}}{\mathrm{VIN}})$$

Where VOUT is the output voltage, VIN is the input voltage, fs is the switching frequency and ΔIL is the peak-to-peak inductor ripple current.

Choose an inductor that will not saturate under the maximum inductor peak current. With load current Iload, the peak inductor current can be calculated by:

$$\mathrm{Ip} = \mathrm{Iload} + \frac{\mathrm{VOUT}}{2\ \mathrm{x}\ \mathrm{fs}\ \mathrm{x}\ \mathrm{L1}}\ \mathrm{x}\ (1 - \frac{\mathrm{VOUT}}{\mathrm{VIN}})$$

5.3 Output Rectifier Diode

The output rectifier diode supplies the current to the inductor when the high side switch is off. To reduce losses due to the diode forward voltage and recovery times, do use a Schottky diode. Choose a diode whose maximum reverse voltage rating is greater than the maximum input voltage, and whose current rating is greater than the maximum load current.

5.4 Input Capacitor

The input current to the buck converter is discontinuous, therefore a capacitor is required to supply the AC current to the buck converter while maintaining the DC input voltage. Do use low ESR capacitors for the best performance. For simplification, choose the input capacitor with RMS current rating greater than half of the maximum load current.

The input capacitor (C1) can be electrolytic, tantalum or ceramic. When using electrolytic or tantalum capacitors, a small, high quality ceramic capacitor, i.e. 0.1µF, should be placed as close to the IC as possible. When using ceramic capacitors, make sure that they have enough capacitance to provide enough charge to prevent excessive voltage ripple at input. The input voltage ripple caused by capacitance can be estimated by:

$$\Delta VIN = \frac{Iload}{fs\ x\ C1}\ x\ \frac{VOUT}{VIN}\ x\ (1 - \frac{VOUT}{VIN})$$

5.5 Output Capacitor

The output capacitor (C2) is required to maintain the DC output voltage. Low ESR capacitors are preferred to keep the output voltage ripple low. The output voltage ripple can be estimated by:

$$\Delta VOUT = \frac{VOUT}{fs\ x\ L}\ x\ (1 - \frac{VOUT}{VIN})\ x\ (Resr + \frac{1}{8\ x\ fs\ x\ C2})$$

Where L is the inductor value and Resr is the equivalent series resistance (ESR) value of the output capacitor. In the case of ceramic capacitors, the impedance at the switching frequency is dominated by the capacitance. The output voltage ripple is mainly caused by the capacitance. For simplification, the output voltage ripple can be estimated by:

$$\Delta VOUT = \frac{VOUT}{8\ x\ fs^2\ x\ L\ x\ C2}\ x\ \left(1 - \frac{VOUT}{VIN}\right)$$

In the case of tantalum or electrolytic capacitors, the ESR dominates the impedance at the switching frequency. For simplification, the output ripple can be estimated by:

$$\Delta VOUT = \frac{VOUT}{fs\ x\ L}\ x\ (1 - \frac{VOUT}{VIN})\ x\ Resr$$

The characteristics of the output capacitor also affect the stability of the regulation system. AXPM11584 can be optimized for a wide range of capacitance and ESR values.

5.6 Compensation Components

AXPM11584 employs current mode control for easy compensation and fast transient response. The system stability and transient response are controlled through the COMP pin. COMP pin is the output of the internal error amplifier. A series capacitor-resistor combination sets a pole-zero combination to control the characteristics of the control system. The DC gain of the voltage feedback loop is given by:

$$Avdc = RL\ x\ Gcs\ x\ Avea\ x\ \frac{VFB}{VOUT}$$

Where Avea is the error amplifier voltage gain; Gcs is the current sense transconductance; RL is the load resistance. The system has two poles. One is due to the compensation capacitor C3 and the output resistor of error amplifier. The other is due to the output capacitor and the load resistor. These poles are located at:

$$fp1 = \frac{Gea}{2\pi\ x\ C3\ x\ Avea}$$

$$fp2 = \frac{1}{2\pi\ x\ C2\ x\ RL}$$

Where Gea is the error amplifier transconductance.

The system has one zero, due to the compensation capacitor C3 and the compensation resistor R3. This zero is located at:

$$fz1 = \frac{1}{2\pi\ x\ C3\ x\ R3}$$

The system may have another zero, if the output capacitor has a large capacitance and/or a high ESR value. The zero, due to the ESR and capacitance of the output capacitor, is located at:

$$\mathrm{fesr} = \frac{1}{2\pi \times \mathrm{C2} \times \mathrm{Resr}}$$

In this case, a third pole set by the compensation capacitor C6 and the compensation resistor R3 is used to compensate the effect of this zero. This pole is located at:

$$\mathrm{fp3} = \frac{1}{2\pi \times \mathrm{C6} \times \mathrm{R3}}$$

The goal of compensation design is to shape the converter transfer function to get a desired loop response. The system crossover frequency where the feedback loop has the unity gain is important. Lower crossover frequencies result in slower transient responses, while higher crossover frequencies could cause system unstable. A good rule of thumb is to set the crossover frequency to approximately one-tenth of the switching frequency.

5.7 High Frequency Operation

The switching frequency can be programmed up to 1.5MHz with an external resistor.

With higher switching frequencies, the inductive reactance of capacitor becomes dominate, so that the equivalent series inductance (ESL) of input/output capacitor determines the input/output ripple voltage at higher switching frequency. As a result of that, high frequency ceramic capacitor is strongly recommended as input decoupling capacitor and output filtering capacitor for high frequency operation.

Layout becomes critical when the device switches at higher frequency. It is essential to place the input decoupling capacitor, rectifying diode and AXPM11584 (VIN pin, SW pin and PGN) as close as possible, with traces that are very short and wide. This can help to greatly reduce the voltage spike on SW node and lower the EMI noise level.

Try to run the feedback trace as far from the inductor and noisy power traces as possible. It is often a good idea to run the feedback trace on the side of the PCB opposite of the inductor with a ground plane separating the two. The compensation components should be placed closed to the device. Do not place the compensation components close to or under high dv/dt SW node, or inside the high di/dt power loop. If you must do so, the proper ground plane must be in place to isolate those. Switching loss is expected to be increased at high switching frequency. To help improve the thermal conduction, a grid of thermal vias can be created right under the exposed pad. It is recommended that they be small so that the hole is essentially filled up during the plating process, thus aiding conduction to the other side. Too large a hole can cause ‘solder wicking’ problems during the reflow soldering process.

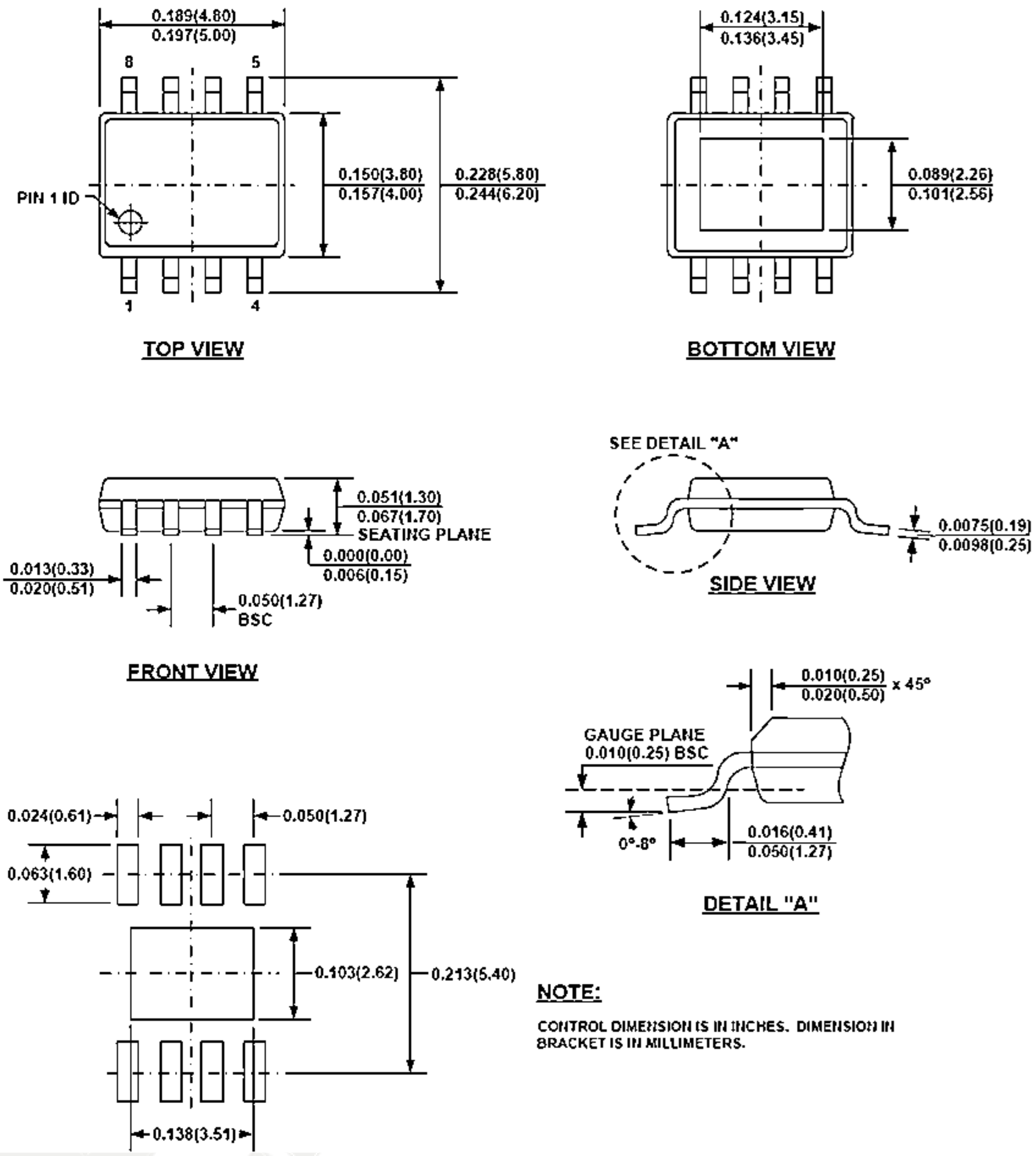
5.8 External Bootstrap Diode

It is recommended that an external bootstrap diode be added when the input voltage is no greater than 5V or the 5V rail is available in the system. This helps improve the efficiency of the regulator. This diode is also recommended for high duty cycle operation (when VOUT/VIN > 65%).

At no load or light load, the converter may operate in pulse skipping mode in order to maintain the output voltage in regulation. Thus, there is less time to refresh the BS voltage. In order to have enough gate voltage under such operating conditions, the difference between VIN and VOUT should be greater than 3V. For example, if the VOUT is set to 3.3V, the VIN needs to be higher than 3.3V + 3V = 6.3V to maintain enough BS voltage at no load or light load. To meet this requirement, EN pin can be used to program the input UVLO voltage to VOUT + 3V.

6 Package Information

Figure 4 SOIC8E Mechanical Data and Package Dimensions



7 Revision History

Table 6 Document Revision History

Date	Version	Description
May 2020	1.00	First version.