

AXPA17388

4 x 45W MOSFET Quad Bridge Power Amplifier

Datasheet — Nov 2022



Description

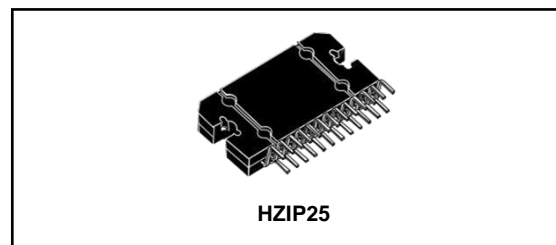
AXPA17388 is a quad bridge class AB car radio audio power amplifier designed in BCD (Bipolar, CMOS, DMOS) technology with a fully complementary P-Channel/N-Channel output structure. It has a rail to rail output voltage swing, high output current and low saturation losses, giving it an excellent distortion performance. AXPA17388 can operate down to 6V for low voltage operation to achieve 'start-stop' battery profile during engine stop enabling reduction in overall emissions.

Features

- Multipower BCD technology with DMOS MOSFET output power stage
- Hi-Fi class low distortion
- Low output noise
- High immunity to RF noise injection
- Standby function
- Mute function
- Auto-mute at min. supply voltage detection
- Low external component count
 - No external compensation
 - No bootstrap capacitors
- Internally fixed gain (26dB)
- Capable to operate down to 6V (e.g. “start-stop”)
- High output power capability:
 - 4 x 45W/4Ω Max.
 - 4 x 25W/4Ω @ 14.4V, 1kHz, 10%
- Protections:
 - Output short circuit to GND, to Vs, across the load
 - Very inductive loads
 - Overrating chip temperature with soft thermal limiter
 - Load dump
 - Fortuitous open GND
 - ESD

Table 1 Device Summary

Order code	Package	Packing
AXPA17388	HZIP25	Tube



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1 Block Diagram and Application Circuits

Figure 1 Block diagram

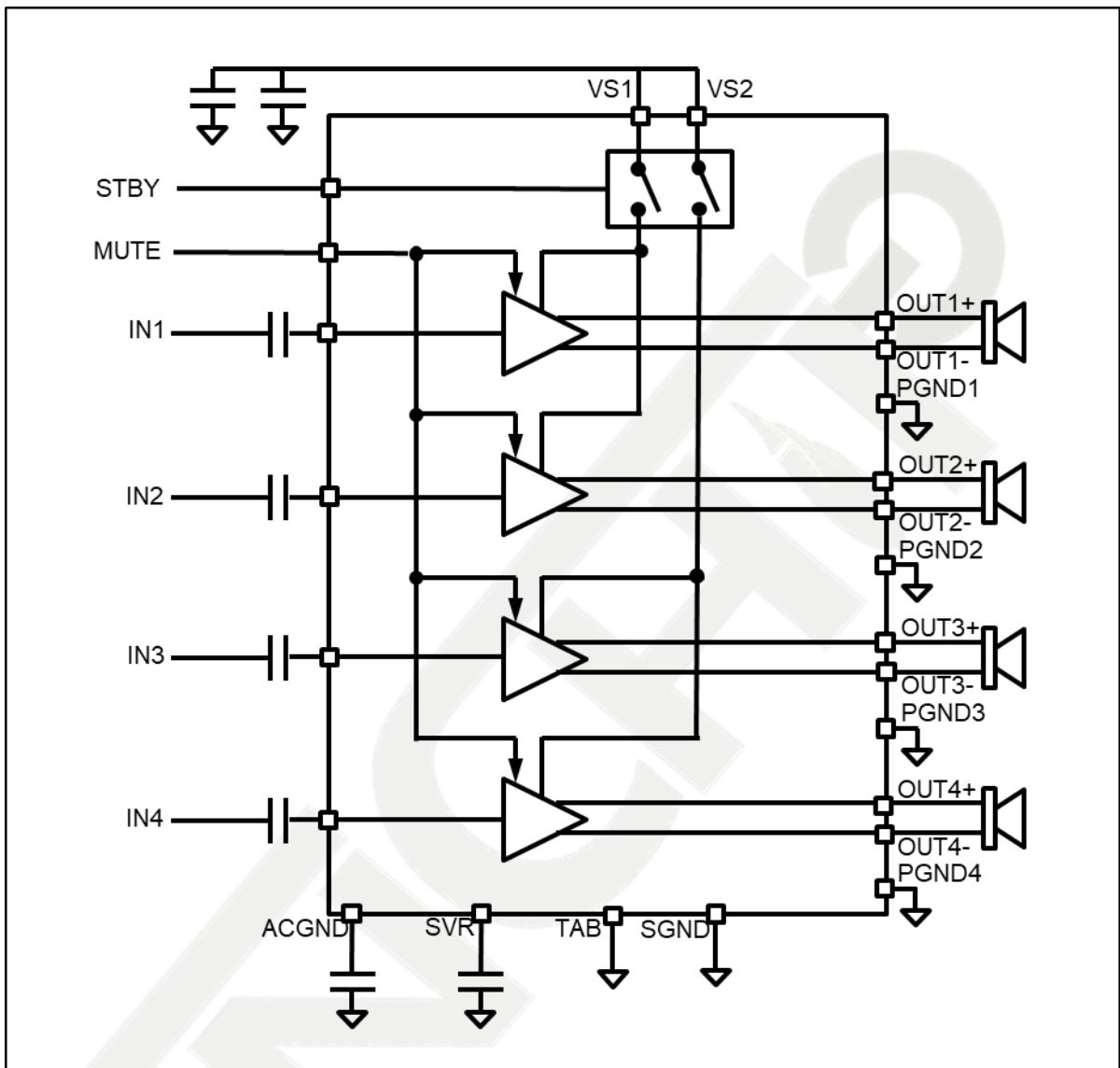
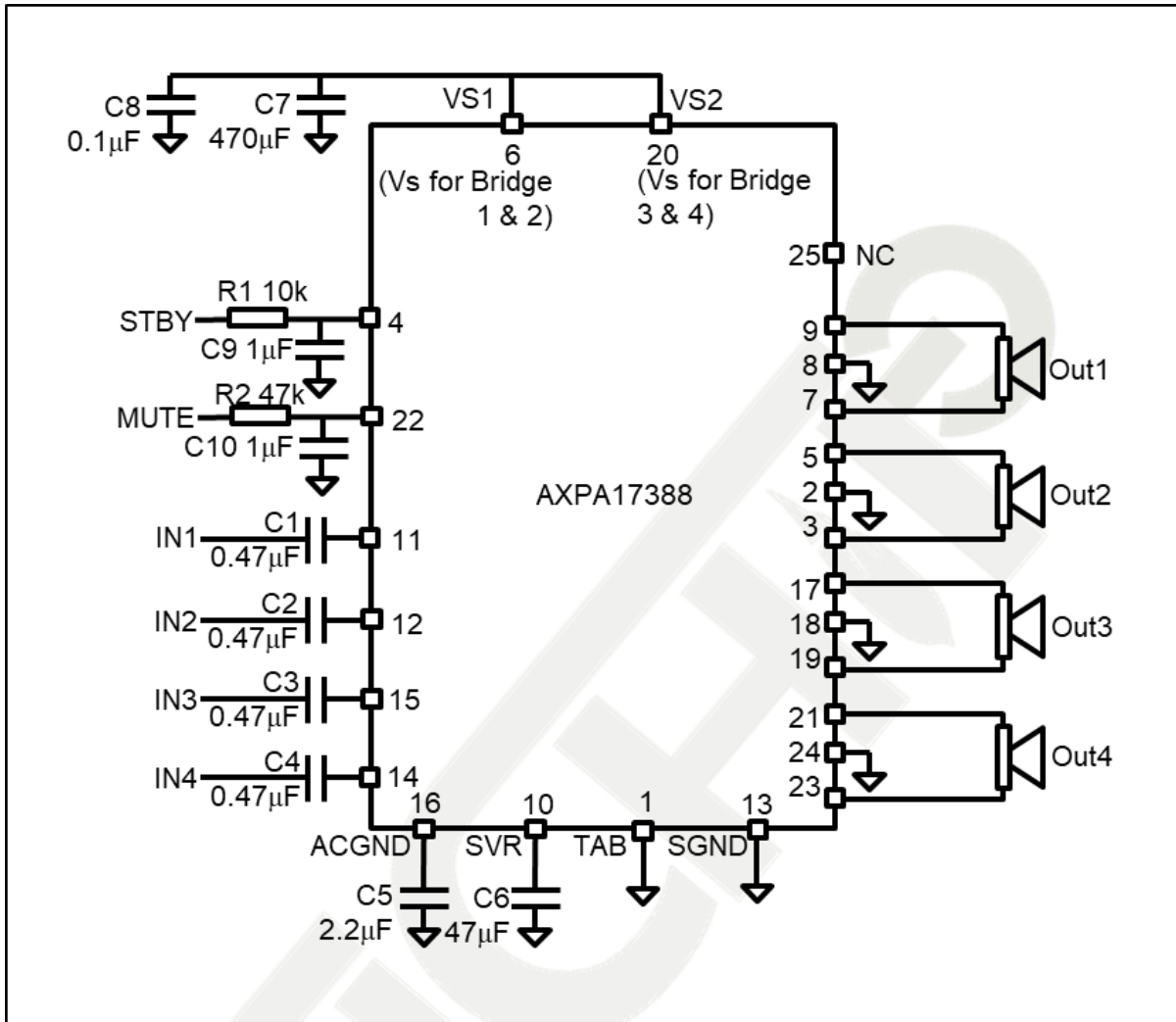


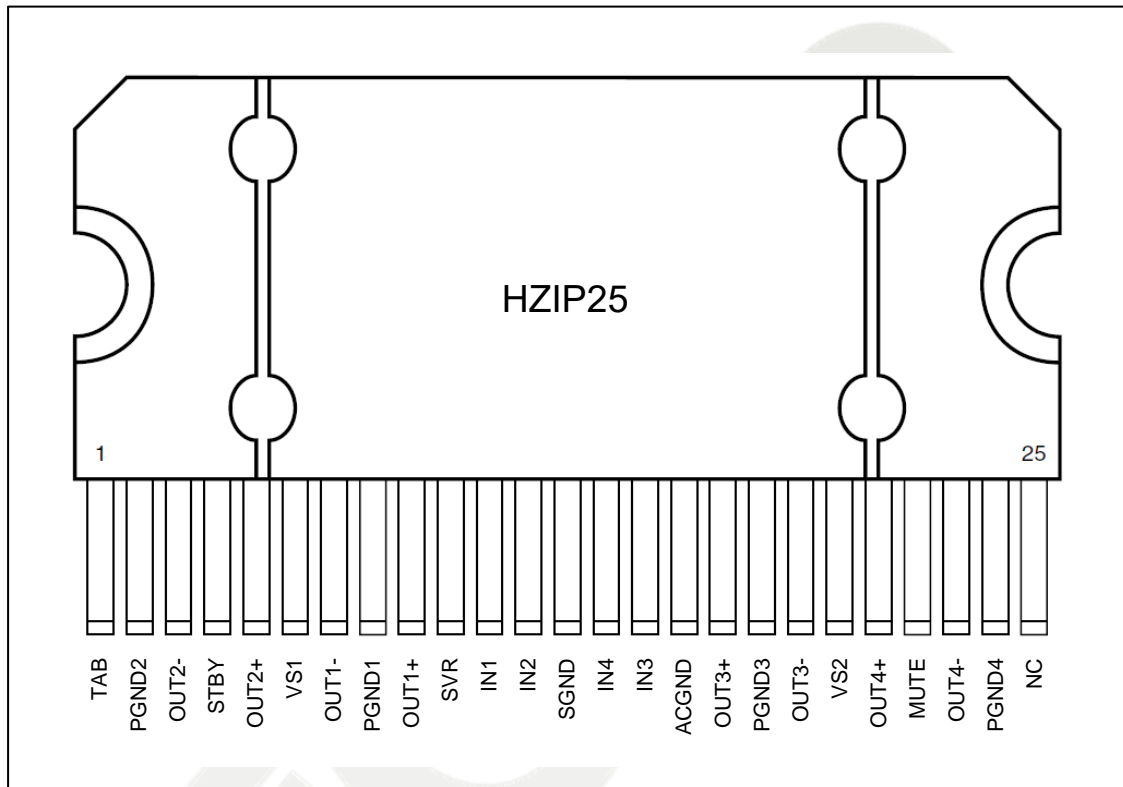
Figure 2 Application circuit



2 Pin Description

2.1 Pin Names

Figure 3 Pin connection



2.2 Pin Functions

Table 2 Pin Functions

Pin number	Pin name	Description
1	TAB	-
2	PGND2	Channel 2, output power ground
3	OUT2-	Channel 2, negative output
4	STBY	Stand-by
5	OUT2+	Channel 2, positive output
6	VS1	Supply voltage
7	OUT1-	Channel 1, negative output
8	PGND1	Channel 1, output power ground
9	OUT1+	Channel 1, positive output
10	SVR	Supply voltage rejection pin
11	IN1	Channel 1, input
12	IN2	Channel 2, input
13	SGND	Signal ground
14	IN4	Channel 4, input
15	IN3	Channel 3, input
16	ACGND	AC ground
17	OUT3+	Channel 3, positive output
18	PGND3	Channel 3, output power ground
19	OUT3-	Channel 3, negative output
20	VS2	Supply voltage
21	OUT4+	Channel 4, positive output
22	MUTE	Mute pin
23	OUT4-	Channel 4, negative output
24	PGND4	Channel 4, output power ground
25	NC	Not Connected

3 Electrical Specifications

3.1 Absolute Maximum Ratings

Table 3 Absolute Maximum Ratings

Symbol	Parameter	Value	Unit
VS	Operating supply voltage	18	V
VS (DC)	DC supply voltage	28	V
VS (pk)	Peak supply voltage (for t = 50ms)	50	V
Io	Output peak current	4.5	A
Ptot	Power dissipation T _{case} = 70°C	80	W
Tj	Junction temperature	150	°C
Tstg	Storage temperature	-55 to 150	°C

3.2 Thermal Data

Table 4 Thermal Data

Symbol	Parameter	Value	Unit
Rth j-case	Thermal resistance junction-to-case Max.	1	°C/W

3.3 Electrical Characteristics

Refer to the test and application diagram, $V_S = 14.4V$; $R_L = 4\Omega$; Signal Generator output impedance $R_g = 600\Omega$; $f = 1kHz$; $T_{amb} = 25^\circ C$; unless otherwise specified.

Table 5 Electrical Characteristics

Symbol	Parameter	Test conditions	Min	Typ	Max	Unit
General characteristics						
V_S	Supply voltage range	-	6	-	18	V
I_q	Quiescent current	$R_L = \infty$	100	180	300	mA
V_{OS}	Output offset voltage	Play mode / Mute mode	-90	-	+90	mV
dV_{OS}	During mute ON/OFF output offset voltage	ITU R-ARM weighted	-10	-	+10	mV
	During standby ON/OFF output offset voltage		-15	-	+15	mV
R_i	Input impedance	-	40	55	70	k Ω
I_{SB}	Standby current consumption	$V_{stby} = 0$	-	-	1	μA
Audio performances						
P_o	Output power	THD = 10%	22	25	-	W
$P_o \text{ max}$	Maximum output power	Square wave input (2Vrms)				
		$V_S = 14.4V$; $R_L = 4\Omega$	37	41	-	W
		$V_S = 15.2V$; $R_L = 4\Omega$		45	-	W
THD	Distortion	$P_o = 4W$	-	0.005	0.05	%
G_v	Voltage gain	-	25	26	27	dB
dG_v	Channel gain unbalance	-	-1	-	+1	dB
e_{No}	Output Noise	"A" Weighted	-	45	-	μV
		Bw = 20Hz to 20kHz	-	70	100	μV
SVR	Supply voltage rejection	$f = 100Hz$; $V_r = 1V_{rms}$	50	65	-	dB
f_{ch}	High cut-off frequency	$P_o = 0.5W$	100	200	-	kHz
CT	Cross talk	$f = 1kHz$ $P_o = 4W$	65	80	-	dB

		$f = 10\text{kHz}$ $P_o = 4\text{W}$	-	65	-	dB
AM	Mute attenuation	$P_o \text{ ref} = 4\text{W}$	80	100	-	dB
Control pin characteristics						
ISTBY	Standby pin current	$V_{\text{stby}} = 1.2\text{V to } 2.6\text{V}$	-	-	1	μA
V _{SB} out	Standby out threshold voltage	(Amp: ON)	2.6	-	-	V
V _{SB} in	Standby in threshold voltage	(Amp: OFF)	-	-	1.2	V
V _M out	Mute out threshold voltage	(Amp: Play)	3.5	-	-	V
V _M in	Mute in threshold voltage	(Amp: Mute)	-	-	1.2	V
V _{AM} in	V _s auto-mute threshold	(Amp: Mute) Att 80dB; $P_o = 4\text{W}$	5	5.4	5.8	V
		(Amp: Play) Att <0.1dB; $P_o = 0.5\text{W}$	-	-	6	V
I _{mute}	Muting pin current	$V_{\text{MUTE}} = 1.2\text{V}$ (Sourced current)	5	9	15	μA

4 Functional Description

4.1 Overview

AXPA17388 is a complementary quad audio power amplifier designed in BCD Technology. Integrated within the AXPA17388 are:

- 4 dependent class AB amplifiers with DMOS Mosfet output stages
- Standby function with STBY pin
- Mute function with MUTE pin
- Circuits fully operational down to 6V, with no pop noise and uninterrupted play during battery transitions.
- Protection circuits for
 - short circuit
 - open circuit
 - over voltage
 - over temperature

It is available in package HZIP25.

4.2 Inputs

AXPA17388's channel inputs are ground-compatible with reference to ACGND. Referring to application circuit (Figure 2), input capacitors of 0.47 μ F will attain a low frequency cut-off of around 16Hz. For best pop noise minimization, input capacitors should be 1/4 of the capacitor connected to ACGND pin.

4.3 Standby and Mute

Standby and Mute functions are controlled by CMOS compatible STBY and MUTE pins.

Control signals for these functions should be coupled to AXPA17388 using a RC circuit (refer to Figure 2 Application Diagram) to damp any sharp transition, preventing unwanted audible transient noise. If not used, an external resistive pull up to V_s should be connected.

4.4 SVR – Supply Voltage Rejection

The SVR pin is set internally to $V_s/4$ and serves as the input voltage reference as well as to generate the $V_s/2$ output reference.

An external capacitor connected to the SVR help in supply voltage ripple rejection and serves 3 functions:

1. Start-up time
2. Shut-down time
3. Pop noise free transitions.

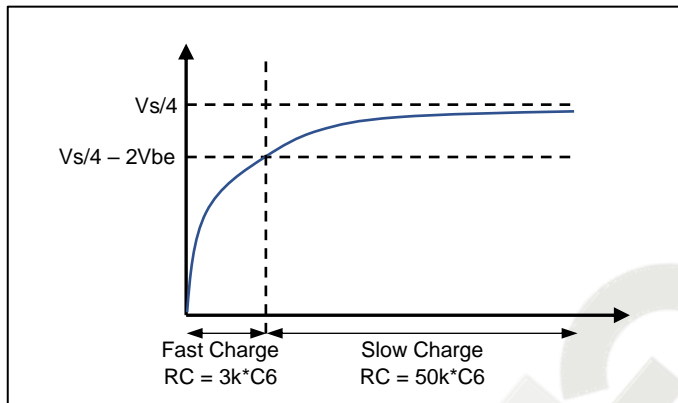
A minimum capacitance value of 10 μ F is recommended.

Upon STBY going beyond the 2.6V threshold, the SVR pin is charged for normal operation.

The Start-up profile time constant is determined by an internal R coupled with the external capacitor. A 2-step profile is designed with a fast charge of 3k Ω from 0 to $V_s/4-2V_{be}$ voltage and thereafter a slower charge through 50k Ω to $V_s/4$ voltage.

A time constant slower than 2.5V/ms is recommended for pop-free transitions.

Figure 4 SVR charge diagram



Proper sequencing of the MUTE and STBY can ensure no audible noise during transition. Placing the amplifier in Mute prior to the device going into or coming out from Standby will ensure no audible noise in the transition.

4.5 Operation Modes

4.5.1 Low Voltage Operation

In the effort to reduce emissions of polluting substances, OEM specifications dictate that the car engine automatically stops when the car is stopping at traffic lights. AXPA17388 can meet this operation requirement.

It provides for continuous operation when the battery falls as low as 6V, remaining fully operational. The output power is however reduced accordingly to the available voltage supply. Upon battery voltage dropping below 6V, a proper sequencing is performed with amplifier first fast muted and then the SVR capacitor discharged. On returning to above 6V, the amplifier restarts.

4.5.2 Cranks

AXPA17388 has excellent performance on worst case cranks profile from 16V to 6V, continuing to play and without producing any pop noise.

It can sustain operation for battery cranking curves shown below:

Figure 5 Battery cranking curve example 1

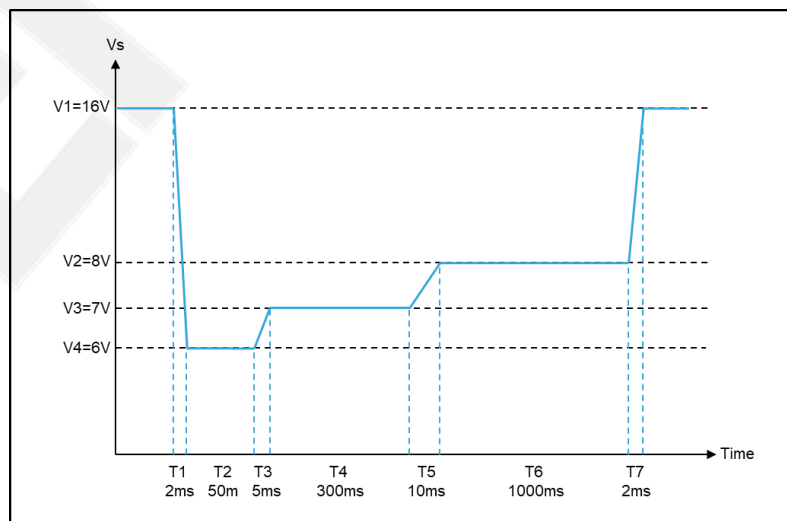
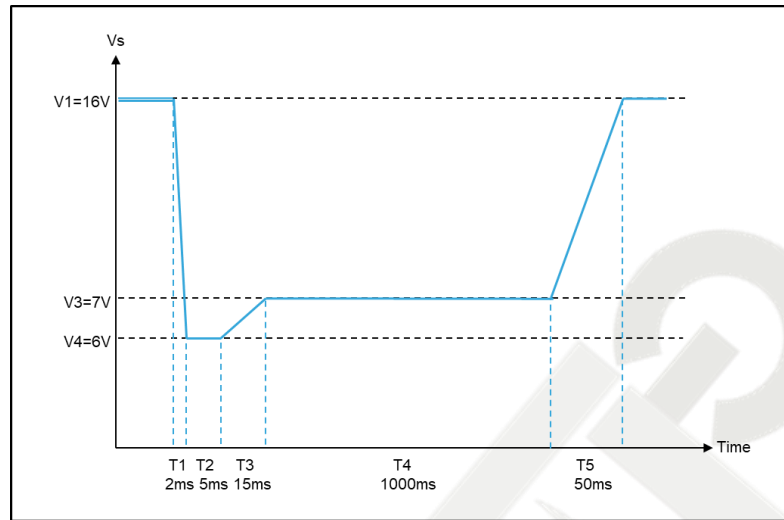


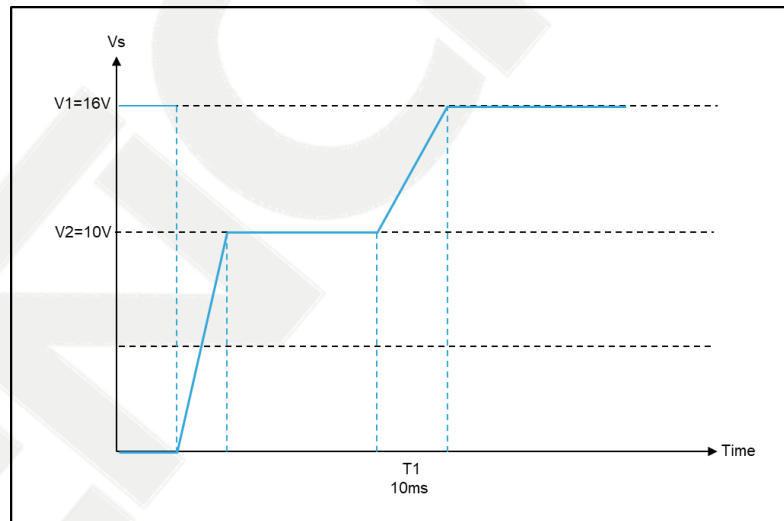
Figure 6 Battery cranking curve example 2



4.5.3 Advanced battery management (hybrid vehicles)

For sudden spikes in battery voltage, as in the case of Hybrid vehicles engine ignition, AXPA17388 can handle such situations of 16V in 10ms spikes without any pop noise and interruptions.

Figure 7 Upwards fast battery transitions diagram



4.6 Protection

4.6.1 Short circuits

AXPA17388 detects for short circuit under the conditions of:

1. Short to ground
When detected, the outputs are put into tristate high impedance. The device will only revert to normal operation when short is removed. This is determined by detecting the output voltage returning to internally set limits.
2. Short to V_s
When detected, the outputs are put into tri-state high impedance. The device will only revert to normal operation when the short is removed. This is determined by detecting the output voltage returning to internally set limits.
3. Short across the load
This is determined by sensing an over current at the outputs. The outputs are then put into a high impedance protection mode for $100\mu s$. The short is repeated checked every $100\mu s$. If the short is removed, the amplifier returns to normal operation, otherwise high impedance state is maintained.

4.6.2 Open circuit Operation

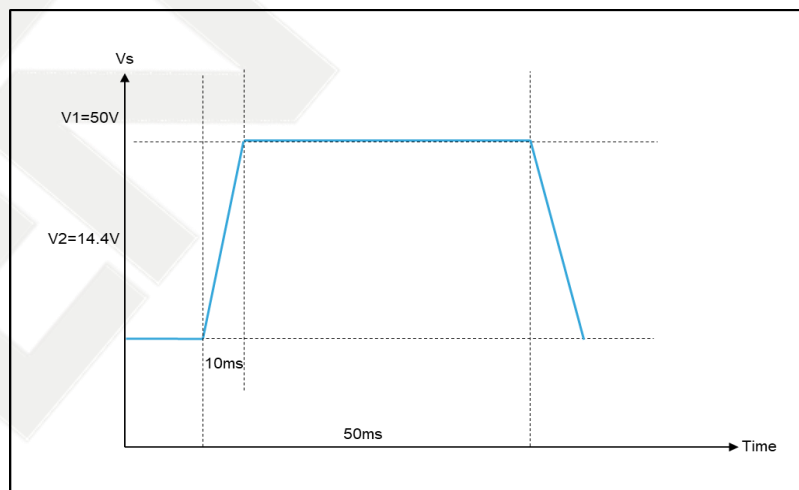
When there is an open load condition, no damage will occur. AXPA17388 will continue to play.

4.6.3 Over-voltage and load dump

AXPA17388 is designed to detect over voltage of beyond 19V. When detected, the amplifier outputs go into a high impedance state preventing damage. Normal play operations are reverted when V_s returns to the acceptable range.

The robustness of the design allows for protection against load dumps surges of as high as 50V with 5ms rise time and 50ms duration.

Figure 8 Load dump protection diagram



4.6.4 Thermal protection

Thermal warning is activated at T_j of $140^\circ C$. If T_j rise continues and reaches $150^\circ C$, a slow mute is then activated to reduce output power and dissipation. On reaching T_j of $170^\circ C$, the amplifier will be shutdown to prevent damage.

4.7 Heat sink definition

The power dissipation and temperature generated by the heat dissipation is governed by the following equation.

$$P_d * (R_{thj\sim case} + R_{thc\sim amb}) = T_j - T_a$$

P_d = Power dissipation of amplifier (W)

$R_{thj\sim case}$ = Thermal resistance from silicon junction to the package casing. ($^{\circ}\text{C}/\text{W}$)

$R_{thc\sim amb}$ = Thermal resistance from case to ambient ($^{\circ}\text{C}/\text{W}$)

T_j = Silicon junction operating temperature ($^{\circ}\text{C}$)

T_a = Ambient Temperature. ($^{\circ}\text{C}$)

Example:

$P_d = 25\text{W}$

$R_{thj\sim case} = 1^{\circ}\text{C}/\text{W}$

$T_j = 150^{\circ}\text{C}$

$T_a = 70^{\circ}\text{C}$

$R_{thc\sim amb} = 2.2^{\circ}\text{C}/\text{W}$

The heatsink need to be designed to have thermal resistance of $2.2^{\circ}\text{C}/\text{W}$ or lower to avoid overheating and thermal shutdown.

5 Package Information

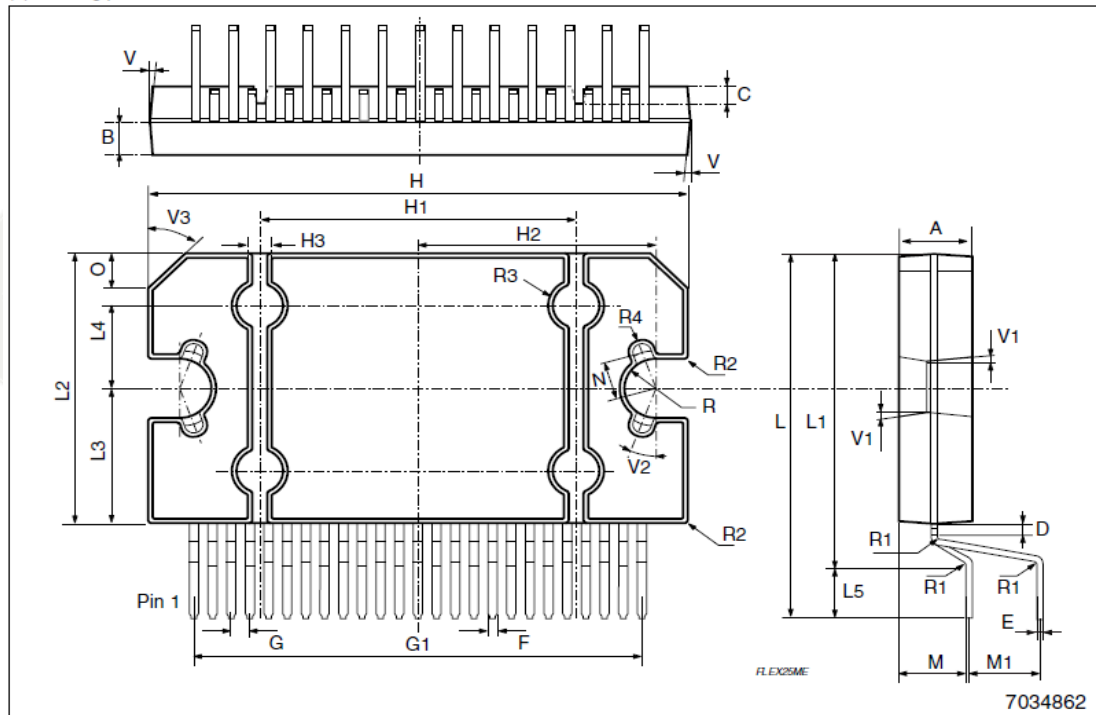
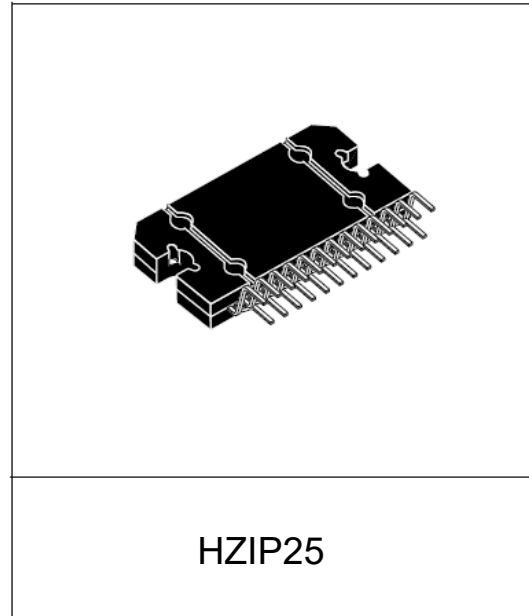
5.1 Package Dimension

Figure 9 HZIP25 vertical mechanical data and package dimensions

DIM.	mm			inch		
	MIN.	TYP.	MAX.	MIN.	TYP.	MAX.
A	4.45	4.50	4.65	0.175	0.177	0.183
B	1.80	1.90	2.00	0.070	0.074	0.079
C		1.40			0.055	
D	0.75	0.90	1.05	0.029	0.035	0.041
E	0.37	0.39	0.42	0.014	0.015	0.016
F (1)			0.57			0.022
G	0.80	1.00	1.20	0.031	0.040	0.047
G1	23.75	24.00	24.25	0.935	0.945	0.955
H (2)	28.90	29.23	29.30	1.139	1.150	1.153
H1		17.00			0.669	
H2		12.80			0.503	
H3		0.80			0.031	
L (2)	22.07	22.47	22.87	0.869	0.884	0.904
L1	18.57	18.97	19.37	0.731	0.747	0.762
L2 (2)	15.50	15.70	15.90	0.610	0.618	0.626
L3	7.70	7.85	7.95	0.303	0.309	0.313
L4		5			0.197	
L5		3.5			0.138	
M	3.70	4.00	4.30	0.145	0.157	0.169
M1	3.60	4.00	4.40	0.142	0.157	0.173
N		2.20			0.086	
O		2			0.079	
R		1.70			0.067	
R1		0.5			0.02	
R2		0.3			0.12	
R3		1.25			0.049	
R4		0.50			0.019	
V				5° (Typ.)		
V1				3° (Typ.)		
V2				20° (Typ.)		
V3				45° (Typ.)		

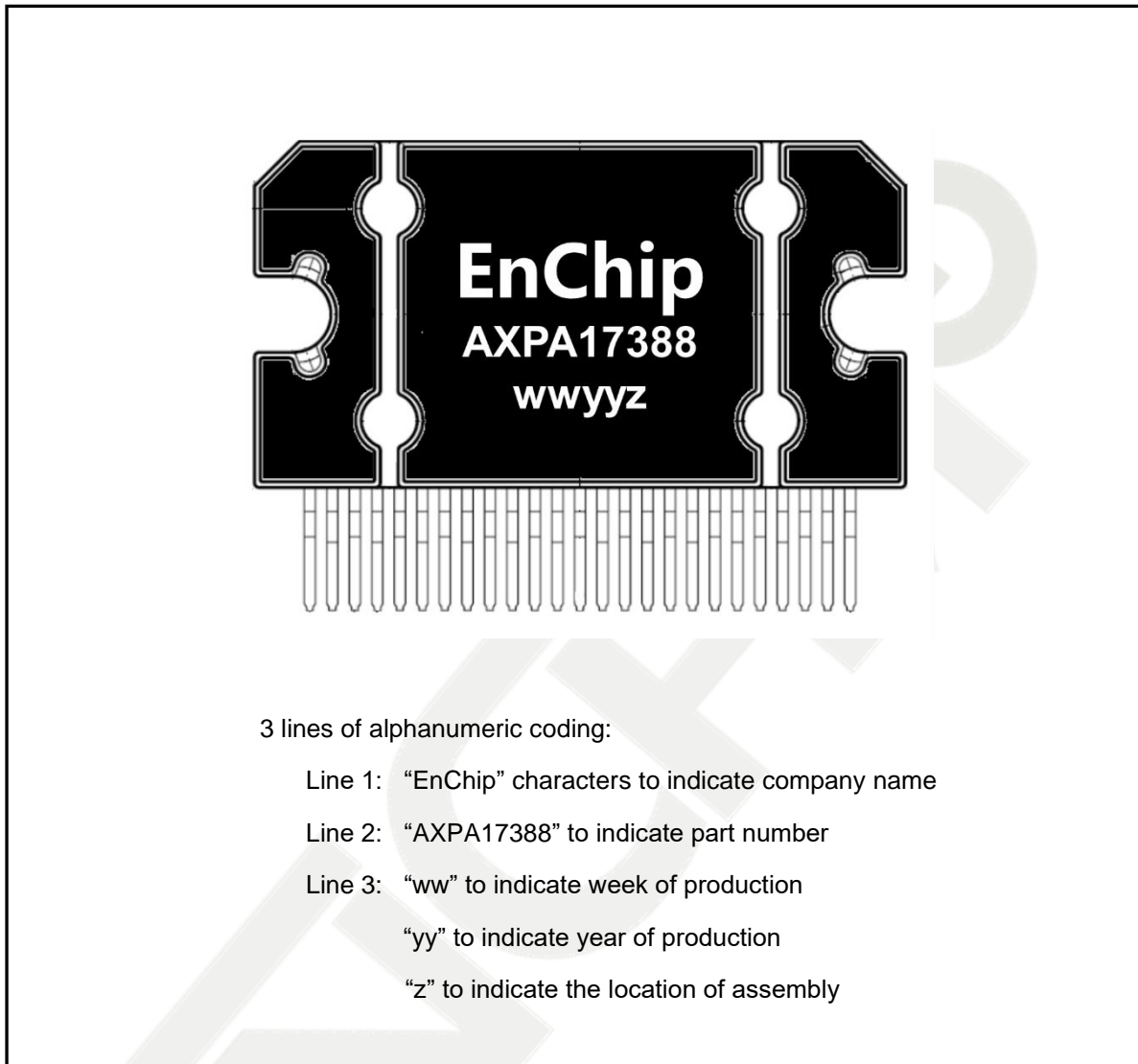
(1): dam-bar protusion not included
 (2): molding protusion included

OUTLINE AND
MECHANICAL DATA



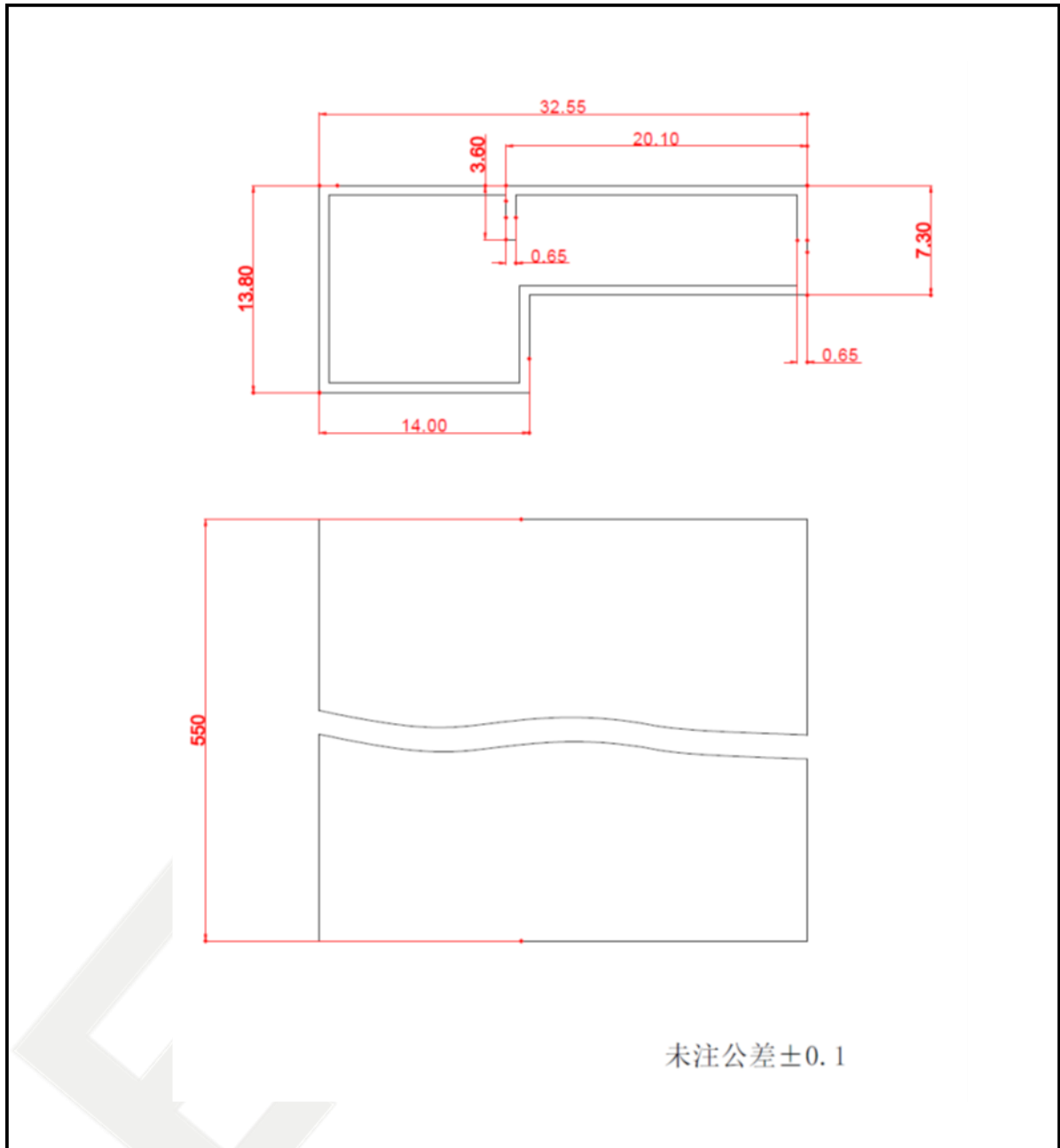
5.2 Marking Information

Figure 10 HZIP25 Marking Information



6 Packing Information

Figure 11 Tube Packing Information



7 Revision History

Table 6 Document Revision History

Date	Version	Description
May 2020	1.00	First Version.
Jul 2021	1.01	Amended pinout typo and removed Clip Detect and DC Offset Detection.
Jun 2022	1.02	Added in Marking and Packaging information.
Nov 2022	1.03	Revised Coupling Capacitors in Application Diagram