

AXOP32062/4/S

20V RRIO Operational Amplifiers
(Dual/Quad)



Datasheet – May 2023

Description

The AXOP32062 (dual), and AXOP32064 (quad) are dual and quad mid voltage (2V to 20V) operational amplifiers (opamps) with rail-to-rail input and output swing capabilities. These devices are very suitable for applications where high voltage operation, a small footprint, and high capacitive load drive are required. AXOP32062S and AXOP32064S are with Shutdown function.

Features

- Supply voltages from 2V to 20V
- Excellent THD+N 96dB
- Excellent SNR 105dB
- Rail-to-rail input and output
- Low input offset voltage: ±1mV typ
- Unity-gain bandwidth: 25MHz
- Low quiescent current (per opamp): 750µA typ @20V
- Easier to stabilize with higher capacitive load due to resistive open-loop output impedance
- Shutdown function (AXOP32062S and AXOP32064S)

Applications

- Infotainment system
- HVAC: heating, ventilating, and air conditioning
- Industrial control
- Test equipment
- Portable Equipment
- Active filters
- Data acquisition system

Table 1 Device Summary

Order code	Package	Packing	MOQ
AXOP32062A	eSOP8	Reel	2500
AXOP32062B	DFN8	Reel	3000
AXOP32062C	SOP8	Reel	4000
AXOP32062D	SOT23-8L	Reel	3000
AXOP32062E	DIP8	Tube	2000
AXOP32062SA	DFN10	Reel	5000
AXOP32062SB	SSOP10	Reel	2500
AXOP32064A	QFN14	Reel	6000
AXOP32064B	TSSOP14	Reel	3000
AXOP32064C	SOP14	Reel	2500
AXOP32064SA	QFN16	Reel	6000
AXOP32064SB	SOP16	Reel	4000



Contents

Description.....	1
Features.....	1
Applications	1
1 Block Diagram and Application Circuit.....	4
2 Pin Description	5
2.1 AXOP32062A/B/C/D/E Pinouts.....	5
2.2 AXOP32062SA/B Pinouts.....	6
2.3 AXOP32064A/B/C Pinouts	7
2.4 AXOP32064SA/B Pinouts.....	8
3 Electrical Specifications.....	9
3.1 Absolute Maximum Ratings	9
3.2 Thermal Data.....	9
3.3 ESD.....	9
3.4 Electrical Characteristics	10
3.5 Typical Electrical Characteristics	12
4 Functional Description.....	15
4.1 Overview	15
4.2 Rail to Rail Input	15
4.3 Rail to Rail Output	15
4.4 Overload Recovery.....	15
4.5 Shutdown	15
5 Package Information	16
5.1 Package Dimensions.....	16
5.2 Marking Information.....	28
6 Packing Information.....	34
7 Revision History	35

List of Figures

Figure 1 Block Diagram.....	4
Figure 2 Typical Application Circuit	4
Figure 3 AXOP32062A/B/C/D/E Pinouts	5
Figure 4 AXOP32062SA/B Pinouts	6
Figure 5 AXOP32064A/B Pinouts.....	7
Figure 6 AXOP32064SA/B Pinouts	8
Figure 7 Vos Distribution.....	12
Figure 8 Vos vs Input Common Mode Voltage	12
Figure 9 Vos vs Vs.....	12
Figure 10 Iq (per opamp) vs Input Common Mode Voltage	13
Figure 11 Iq (per opamp) vs Vs.....	13
Figure 12 THD+N vs Frequency.....	13
Figure 13 Large Signal Step Response.....	14
Figure 14 Step Response @Vs=20V, CL=1nF	14
Figure 15 eSOP8 Mechanical Data and Package Dimensions	16
Figure 16 DFN8 Mechanical Data and Package Dimensions	17
Figure 17 SOP8 Mechanical Data and Package Dimensions	18
Figure 18 SOT23-8L Mechanical Data and Package Dimensions	19
Figure 19 DIP8 Mechanical Data and Package Dimensions.....	20
Figure 20 DFN10 Mechanical Data and Package Dimensions	21
Figure 21 SSOP10 Mechanical Data and Package Dimensions.....	22
Figure 22 QFN14 Mechanical Data and Package Dimensions	23
Figure 23 TSSOP14 Mechanical Data and Package Dimensions.....	24
Figure 24 SOP14 Mechanical Data and Package Dimensions	25
Figure 25 QFN16 Mechanical Data and Package Dimensions	26
Figure 26 SOP16 Mechanical Data and Package Dimensions	27
Figure 27 eSOP8 Marking Information	28
Figure 28 DFN8 Marking Information	28
Figure 29 SOP8 Marking Information	29
Figure 30 SOT23-8L Marking Information	29
Figure 31 DIP8 Marking Information.....	30
Figure 32 DFN10 Marking Information	30
Figure 33 SSOP10 Marking Information.....	31
Figure 34 QFN14 Marking Information	31
Figure 35 TSSOP14 Marking Information.....	32
Figure 36 SOP14 Marking Information	32
Figure 37 QFN16 Marking Information	33
Figure 38 SOP16 Marking Information	33
Figure 39 Reel Packing Information	34

List of Tables

Table 1 Device Summary	1
Table 2 Absolute Maximum Ratings	9
Table 3 Thermal Data	9
Table 4 ESD	9
Table 5 Electrical Characteristics	10
Table 6 Document Revision History	35

1 Block Diagram and Application Circuit

Figure 1 Block Diagram

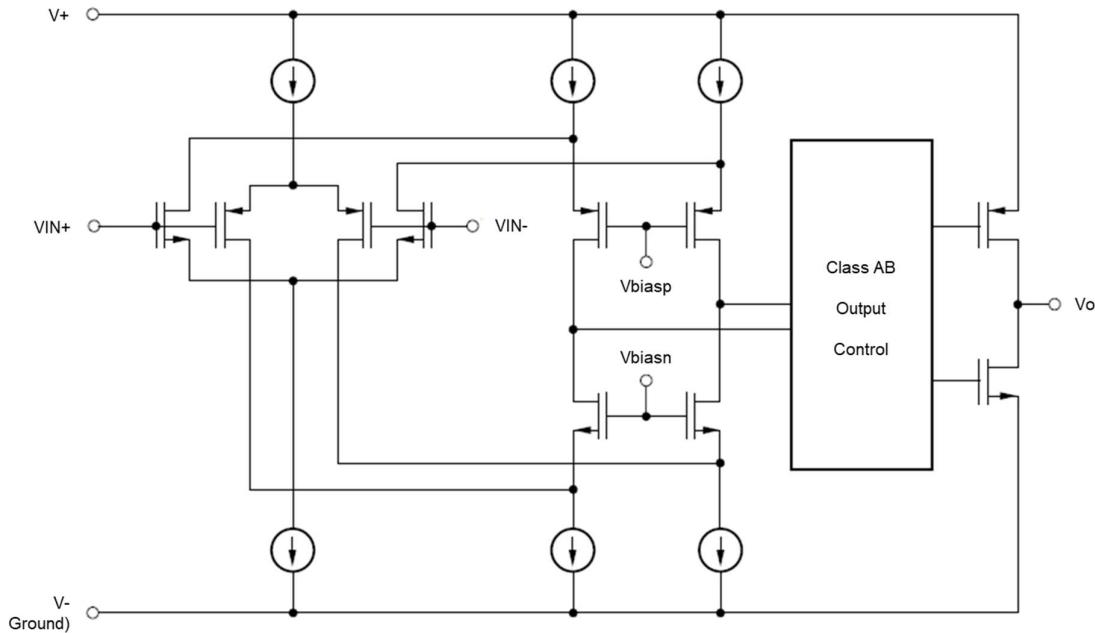
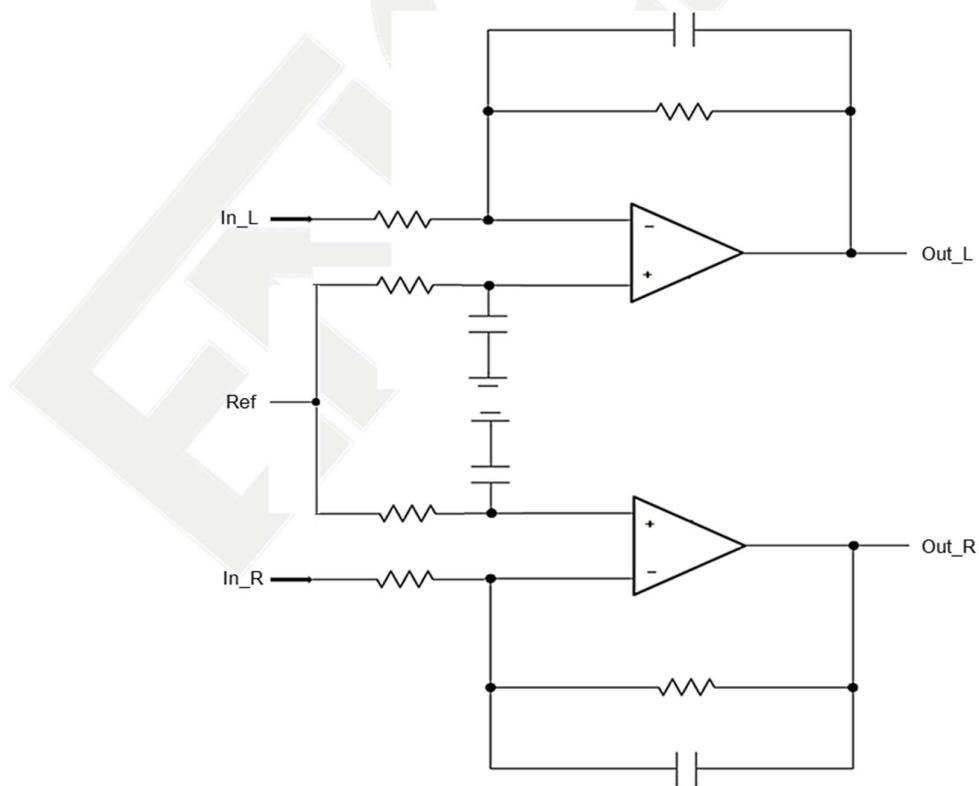


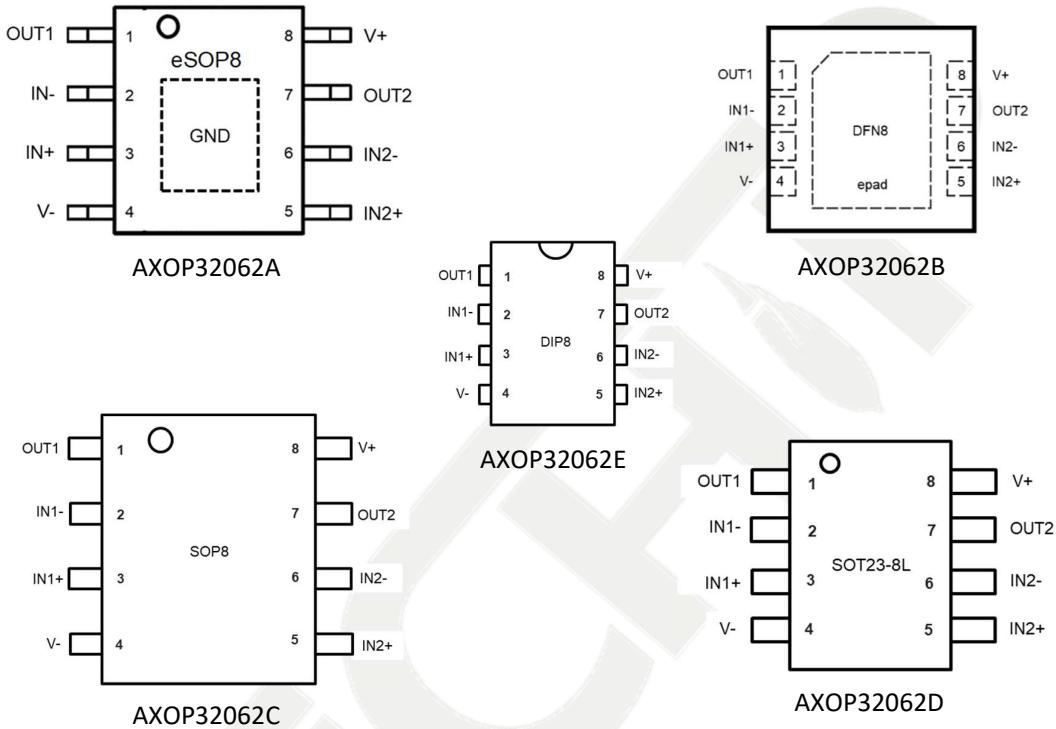
Figure 2 Typical Application Circuit (Stereo Sound Input Amplifier)



2 Pin Description

2.1 AXOP32062A/B/C/D/E Pinouts

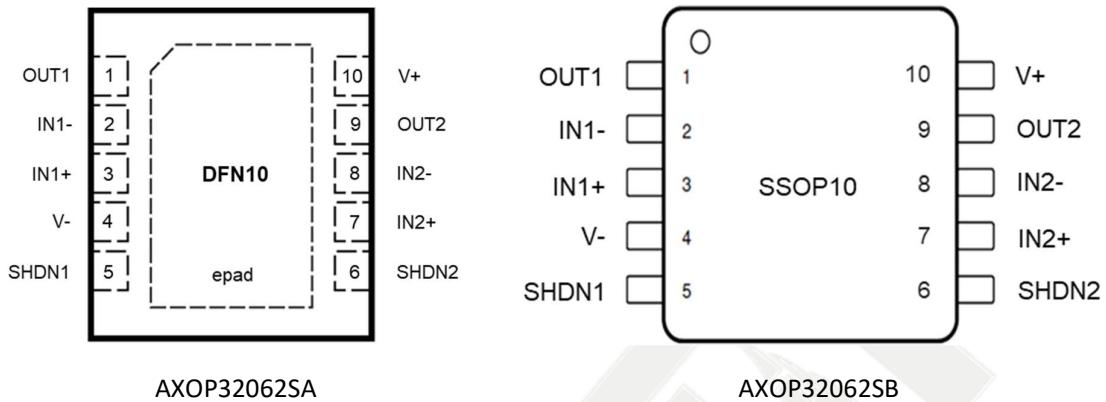
Figure 3 AXOP32062A/B/C/D/E Pinouts



Pin number	Pin name	Description
1	OUT1	Output 1
2	IN1-	Inverting input 1
3	IN1+	Non-inverting input 1
4	V-	Negative supply or ground
5	IN2+	Non-inverting input 2
6	IN2-	Inverting input 2
7	OUT2	Output 2
8	V+	Positive supply

2.2 AXOP32062SA/B Pinouts

Figure 4 AXOP32062SA/B Pinouts



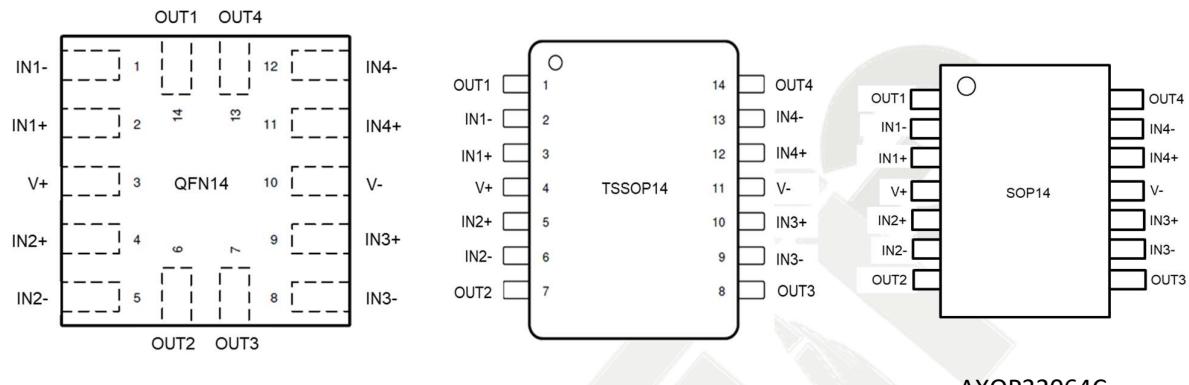
AXOP32062SA

AXOP32062SB

Pin number	Pin name	Description
1	OUT1	Output 1
2	IN1-	Inverting input 1
3	IN1+	Non-inverting input 1
4	V-	Negative supply or ground
5	SHDN1	Shutdown1: "High" = opamp 1 disabled Shutdown1: "Low" = opamp 1 enabled Shutdown1: "Float" = opamp 1 enabled
6	SHDN2	Shutdown2: "High" = opamp 1 disabled Shutdown2: "Low" = opamp 1 enabled Shutdown2: "Float" = opamp 1 enabled
7	IN2+	Non-inverting input 2
8	IN2-	Inverting input 2
9	OUT2	Output 2
10	V+	Positive supply

2.3 AXOP32064A/B/C Pinouts

Figure 5 AXOP32064A/B Pinouts



AXOP32064A

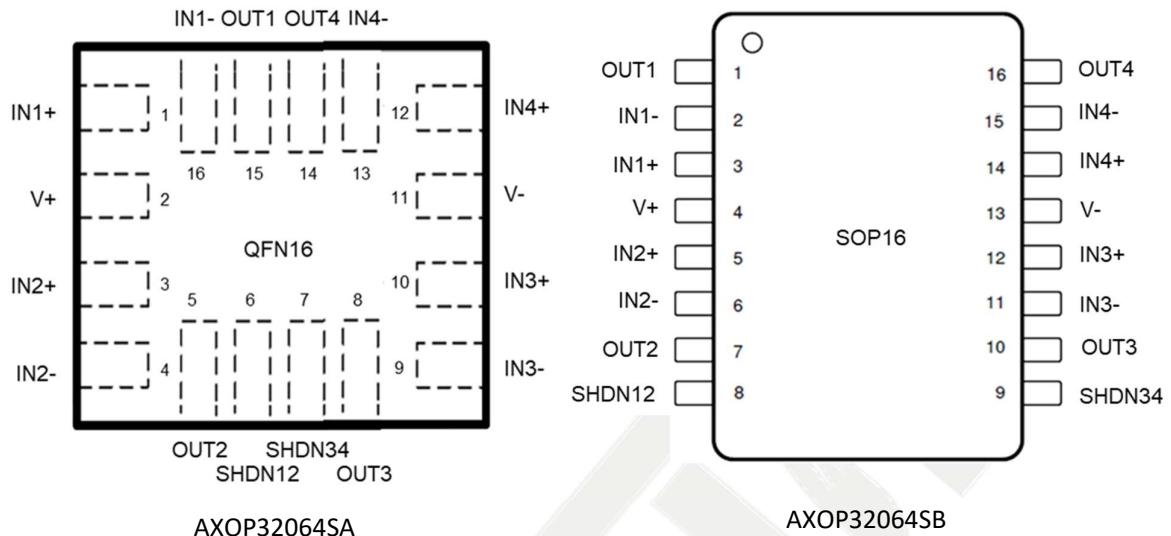
AXOP32064B

AXOP32064C

	AXOP32064A		AXOP32064B/C	
Pin number	QFN14 Pin name	QFN14 Description	TSSOP14/ SOP14 Pin name	TSSOP14 / SOP14 Description
1	IN1-	Inverting input 1	OUT1	Output 1
2	IN1+	Non-inverting input 1	IN1-	Inverting input 1
3	V+	Positive supply	IN1+	Non-inverting input 1
4	IN2+	Non-inverting input 2	V+	Positive supply
5	IN2-	Inverting input 2	IN2+	Non-inverting input 2
6	OUT2	Output 2	IN2-	Inverting input 2
7	OUT3	Output 3	OUT2	Output 2
8	IN3-	Inverting input 3	OUT3	Output 3
9	IN3+	Non-inverting input 3	IN3-	Inverting input 3
10	V-	Negative supply or ground	IN3+	Non-inverting input 3
11	IN4+	Non-inverting input 4	V-	Negative supply or ground
12	IN4-	Inverting input 4	IN4+	Non-inverting input 4
13	OUT4	Output 4	IN4-	Inverting input 4
14	OUT1	Output 1	OUT4	Output 4

2.4 AXOP32064SA/B Pinouts

Figure 6 AXOP32064SA/B Pinouts



	AXOP32064SA		AXOP32064SB	
Pin number	QFN16 Pin name	QFN16 Description	SOP16 Pin name	SOP16 Description
1	IN1+	Non-inverting input 1	OUT1	Output 1
2	V+	Positive supply	IN1-	Inverting input 1
3	IN2+	Non-inverting input 2	IN1+	Non-inverting input 1
4	IN2-	Inverting input 2	V+	Positive supply
5	OUT2	Output 2	IN2+	Non-inverting input 2
6	SHDN12	Shutdown12: "High" = opamp 1&2 disabled	IN2-	Inverting input 2
7	SHDN34	Shutdown34: "High" = opamp 3&4 disabled	SHDN12	Shutdown12: "High" = opamp 1&2 disabled
8	OUT3	Output 3	SHDN34	Shutdown34: "High" = opamp 3&4 disabled
9	IN3-	Inverting input 3	IN3-	Inverting input 3
10	IN3+	Non-inverting input 3	OUT3	Output 3
11	V-	Negative supply or ground	IN3-	Inverting input 3
12	IN4+	Non-inverting input 4	IN3+	Non-inverting input 3
13	IN4-	Inverting input 4	V-	Negative supply or ground
14	OUT4	Output 4	IN4+	Non-inverting input 4
15	OUT1	Output 1	IN4-	Inverting input 4
16	IN1-	Inverting input 1	OUT4	Output 4

3 Electrical Specifications

3.1 Absolute Maximum Ratings

Table 2 Absolute Maximum Ratings

Symbol	Parameter	Value	Unit
V _s	Supply voltage (V+) - (V-)	-0.3 to +27	V
I _{N+} , I _{N-}	Input pin voltage	(V-) - 0.5 to (V+) +0.5	V
O _{UT}	Output pin voltage	(V-) - 0.5 to (V+) +0.5	V
T _j	Junction temperature	150	°C
T _{stg}	Storage temperature	-55 to +150	°C

3.2 Thermal Data

Table 3 Thermal Data

Package	R _{th j-amb}	R _{th j-case}	Unit
eSOP8	60	10	°C/W
DFN8	43	5	°C/W
SOP8	136	77	°C/W
SOT23-8L	184	100	°C/W
DIP8	85	41	°C/W
DFN10	42	6	°C/W
SSOP10	160	45	°C/W
QFN14	47	4	°C/W
TSSOP14	113	62	°C/W
SOP14	106	64	°C/W
QFN16	45	5	°C/W
SOP16	80	30	°C/W

3.3 ESD

Table 4 ESD

Symbol	Parameter	Value	Unit
All pins	ESD (HBM)	±2,000	V

3.4 Electrical Characteristics

For $V_s = (V_+) - (V_-) = 20V$ at $T_a = 25^\circ C$, $R_L = 10k\Omega$ connected to $V_s/2$, $V_{cm} = V_s/2$, and $V_{out} = V_s/2$ (unless otherwise noted).

Table 5 Electrical Characteristics

Symbol	Parameter	Test condition	Min	Typ	Max	Unit
V_s	Supply voltage (V_+) - (V_-)		2		20	V
T_a	Operating ambient temperature		-40		85	°C
Power Supply						
I_q	Quiescent current per amplifier	$V_s=20V$, $I_o=0mA$ all temp		750	900	µA
Offset Voltage						
V_{os}	Input offset voltage			±1	±3	mV
	all temp				±5	mV
dV_{os}/dT	Drift	all temp		±0.5		µV/°C
PSRR	Power-supply rejection ratio	At DC		120		dB
Csep	Channel separation	At DC		120		dB
Input Voltage Range						
V_{cm}	Common mode voltage range	$V_s=2V$ to $20V$	$(V_-)-0.1$		$(V_+)+0.1$	V
CMRR	Common mode rejection ratio	At DC		100		dB
Input Bias Current						
I_b	Input bias current			±0.5		pA
I_{os}	Input offset current			±0.05		pA
Noise						
E_n	Input voltage noise	$f=20Hz$ to $20kHz$		3		µV
Input Capacitance						
C_{id}	Differential			2		pF
C_{ic}	Common mode			4		pF
Open Loop Gain						
A_{ol}	Open loop voltage gain			130		dB
Frequency Response						
GBP	Gain bandwidth product	$G=+1$, $CL=10pF$		25		MHz
Cload	Capacitive load	$G=+1$			1.5	nF
SR	Slew rate	$G=+1$, $CL=100pF$		15		V/µs
Ts	Settling time	To 0.1%, 2V step, $G=+1$, $CL=100pF$		0.3		µs

THD+N	Total harmonic distortion + Noise (3 rd order filter; BW= 80kHz at -3dB.)	V _s =20V, V _{cm} =10V, V _o =1Vrms, G=+1, f=1kHz		96		dB
SNR	Signal to Noise Ratio	V _s =20V, V _{in} =1Vrms, G=+1, f=1kHz		105		dB
Output						
V _o	Voltage output swing from supply rails	RL=10kΩ		40	60	mV
		RL=2kΩ		150	200	
I _{sc}	Short circuit current		±30			mA
		AXOP32062A only eSOP8 package	±100			mA
Shutdown (AXOP32062S and AXOP32064S only)						
I _{qsd}	Quiescent current per amplifier	V _s =2V to 20V, amplifier disabled, SHDN = "High"		30	50	μA
V _{sd}	Shutdown threshold	V _s =2V to 20V, amplifier disabled, SHDN = "High"	4			V
V _{sdl}	Low level shutdown threshold	V _s =2V to 20V, amplifier enabled, SHDN = "Float" or SHDN = "Low"			1	V
t _{on}	Amplifier enable time	V _s =2V to 20V, full shutdown; G=+1, V _o = 0.9×V _s /2, RL connected to V-		10		μs
t _{off}	Amplifier disable time	V _s =2V to 20V, G=+1, V _o =0.1×V _s /2, RL connected to V-		1		μs

Disable time (t_{off}) and enable time (t_{on}) are defined as the time interval between the 50% point of the signal applied to the SHDN pin and the point at which the output voltage reaches the 10% (disable) or 90% (enable) level.

3.5 Typical Electrical Characteristics

Figure 7 Vos Distribution

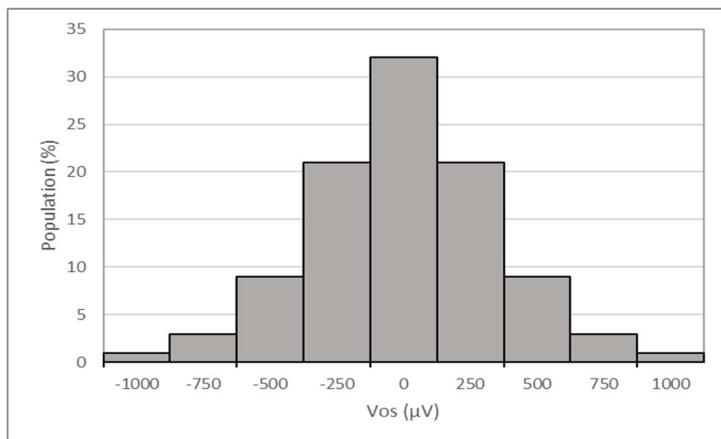


Figure 8 Vos vs Input Common Mode Voltage

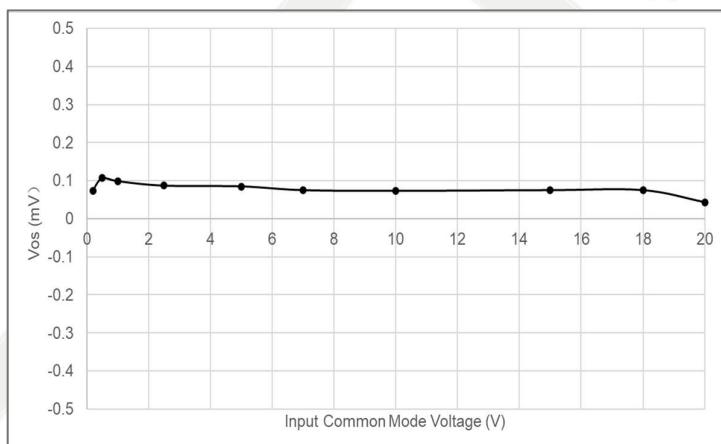


Figure 9 Vos vs Vs

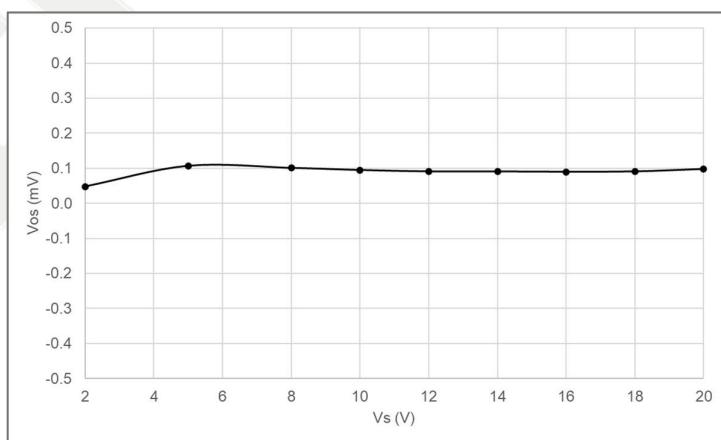


Figure 10 I_q (per opamp) vs Input Common Mode Voltage

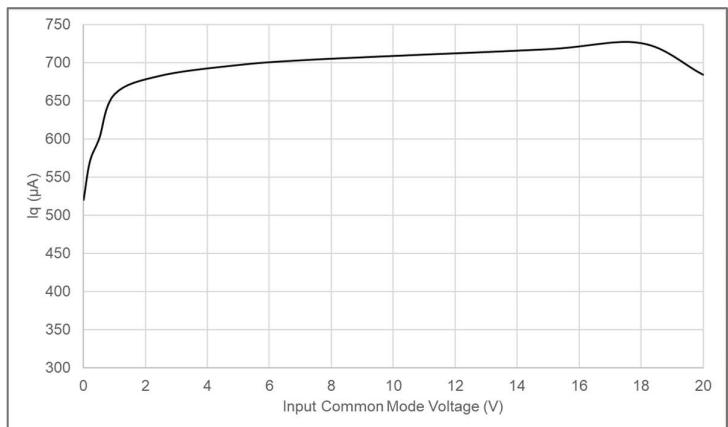


Figure 11 I_q (per opamp) vs V_s

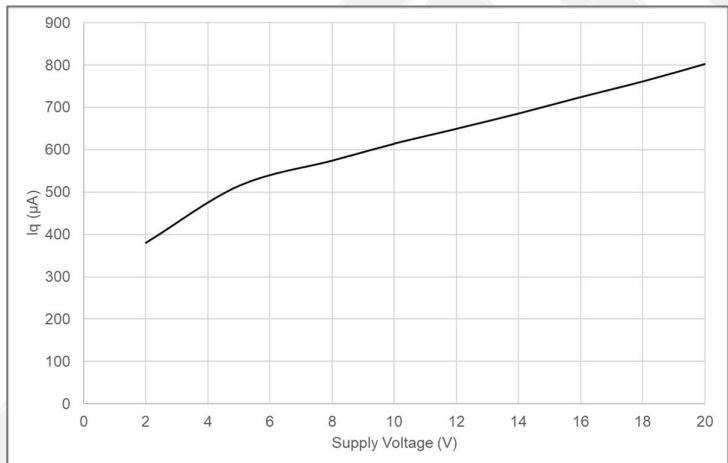


Figure 12 THD+N vs Frequency

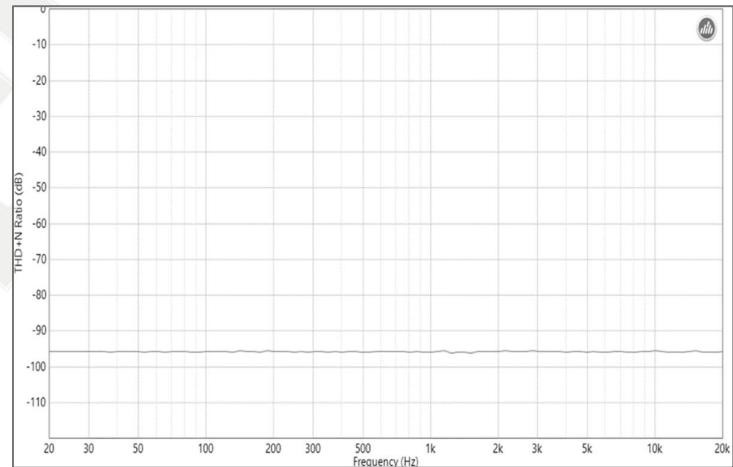


Figure 13 Large Signal Step Response

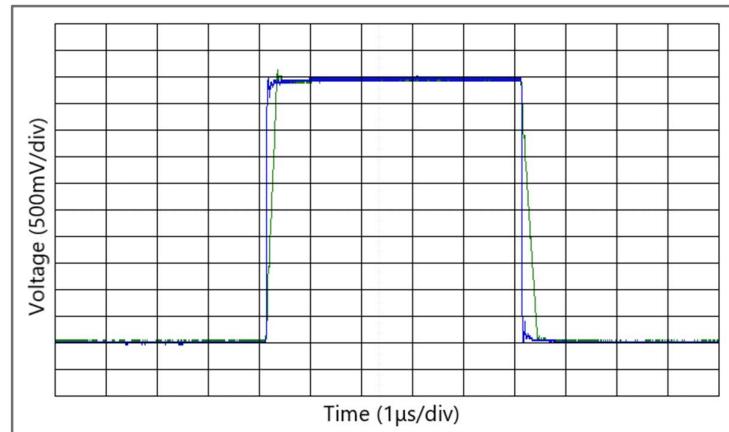
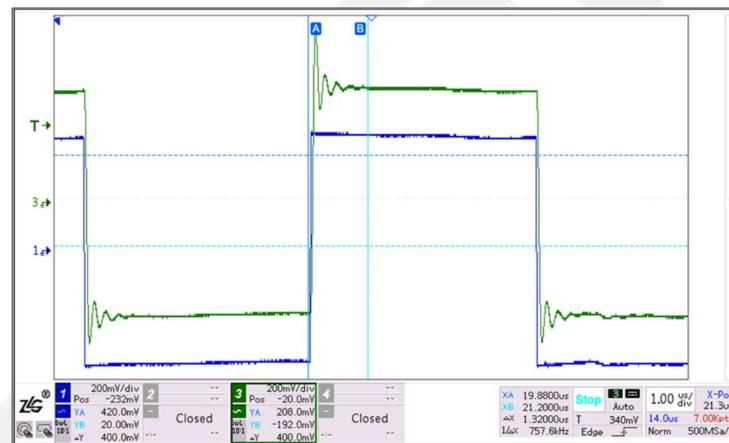


Figure 14 Step Response @Vs=20V, CL=1nF



4 Functional Description

4.1 Overview

The AXOP3206x devices are a family of high voltage, rail-to-rail input and output opamps. These devices operate from 2V to 20V, are unity gain stable, and are designed for a wide range of applications and used in virtually any single supply application.

4.2 Rail to Rail Input

The input common mode voltage range of the AXOP3206x family extends 100mV beyond the supply rails for the full supply voltage range of 2V to 20V. This performance is achieved with a complementary input stage: a N-channel input differential pair in parallel with a P-channel differential pair, as shown in Figure 1. The N-channel pair is active for input voltages close to the positive rail, typically $(V^+)-1.4V$ to 200mV above the positive supply, whereas the P-channel pair is active for inputs from 200mV below the negative supply to approximately $(V^+)-1.4V$. There is a transition region, in which both pairs are on. Within this transition region, PSRR, CMRR, offset voltage, offset drift, and THD can degrade compared to device operation outside this region.

4.3 Rail to Rail Output

Designed as a high voltage operational amplifier, the AXOP3206x series delivers a robust output drive capability. A class AB output stage with common source Mosfets achieves full rail-to-rail output swing capability. For resistive loads of $10k\Omega$, the output swings to within 40mV (typ) of either supply rail, regardless of the applied power supply voltage. Different load conditions change the ability of the amplifier to swing close to the rails.

4.4 Overload Recovery

Overload recovery is defined as the time required for the opamp output to recover from a saturated state to a linear state. The output devices of the opamp enter a saturation region when the output voltage exceeds the rated operating voltage, because of the high input voltage or the high gain. After the device enters the saturation region, the charge carriers in the output devices require time to return to the linear state. After the charge carriers return to the linear state, the device begins to slew at the specified slew rate. The overload recovery time for the AXOP3206x family is approximately 100ns.

4.5 Shutdown

The AXOP3206xS has shutdown function. The amplifiers can be shut down by enabling the respective shutdown pin.

5 Package Information

5.1 Package Dimensions

Figure 15 eSOP8 Mechanical Data and Package Dimensions

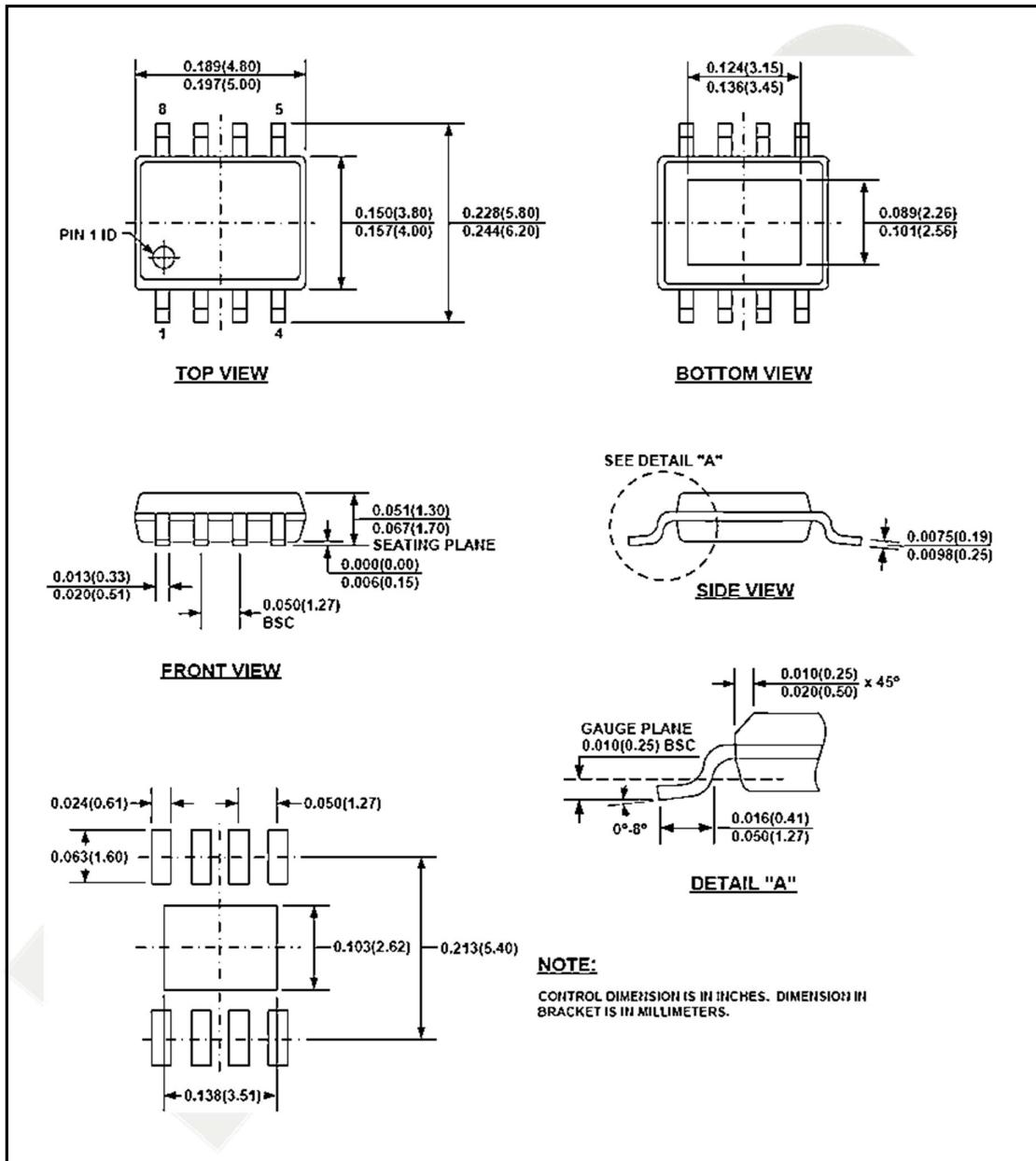


Figure 16 DFN8 Mechanical Data and Package Dimensions

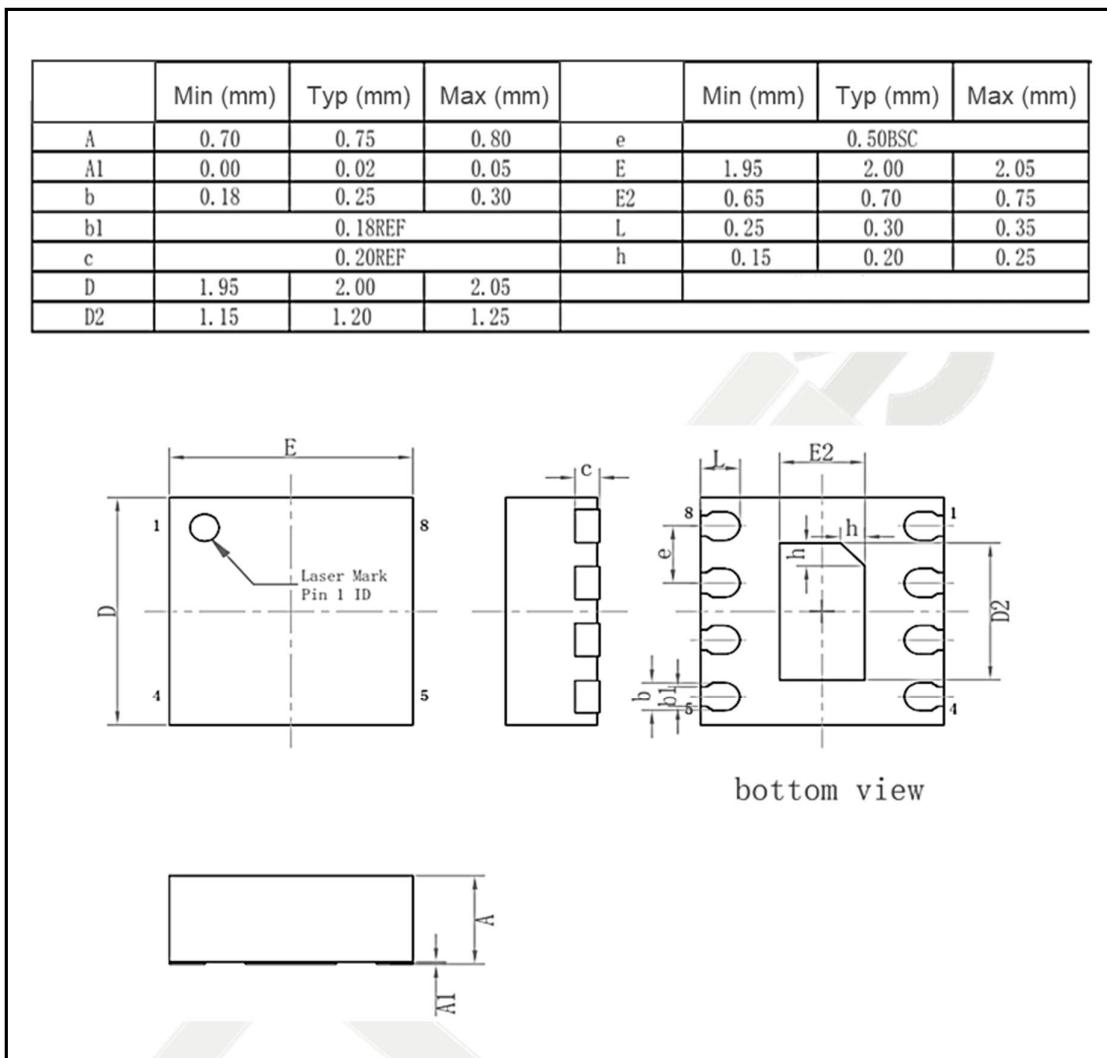


Figure 17 SOP8 Mechanical Data and Package Dimensions

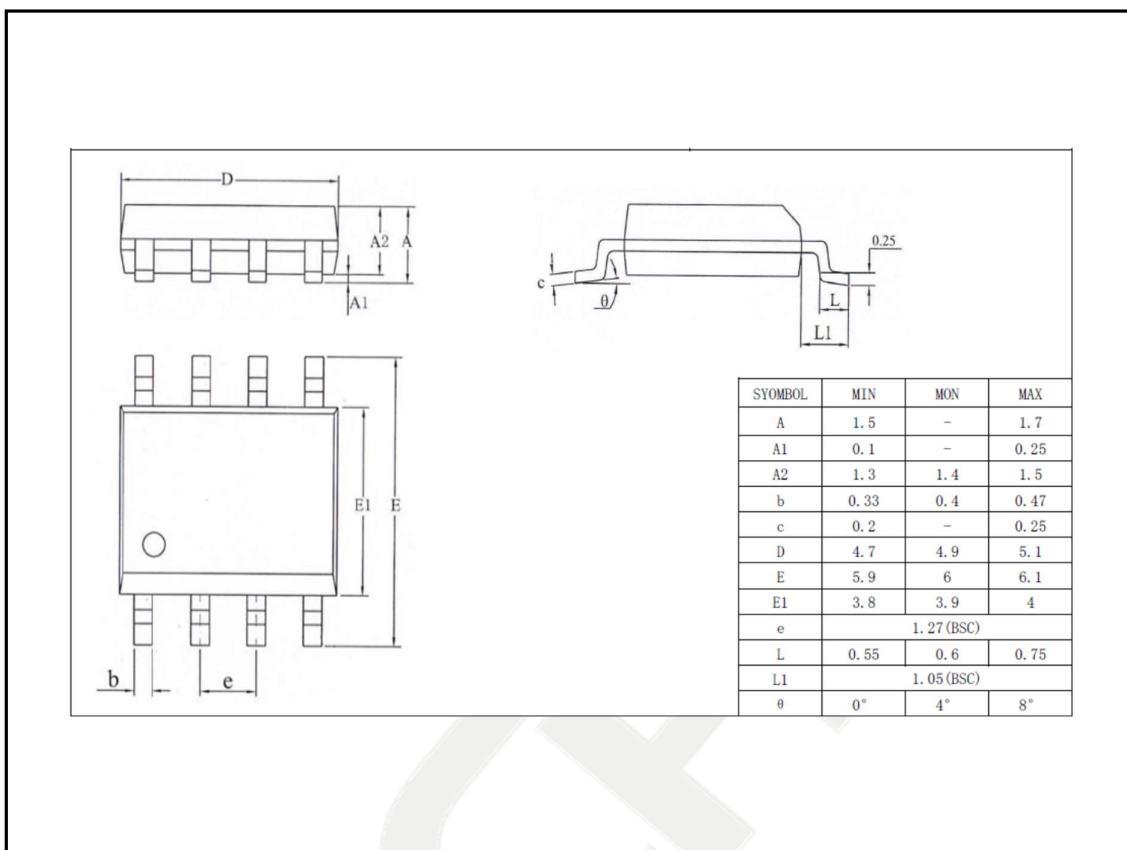


Figure 18 SOT23-8L Mechanical Data and Package Dimensions

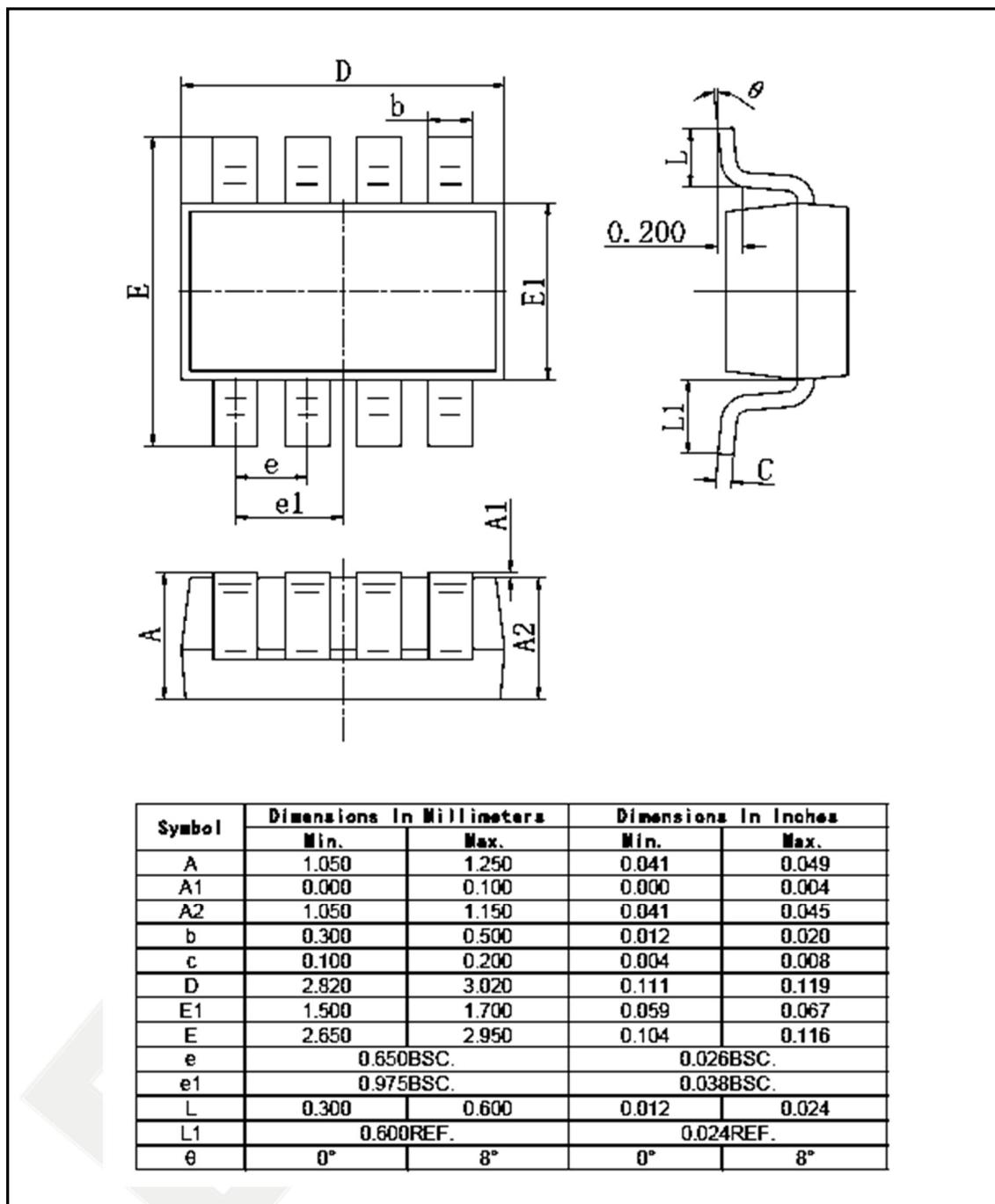


Figure 19 DIP8 Mechanical Data and Package Dimensions

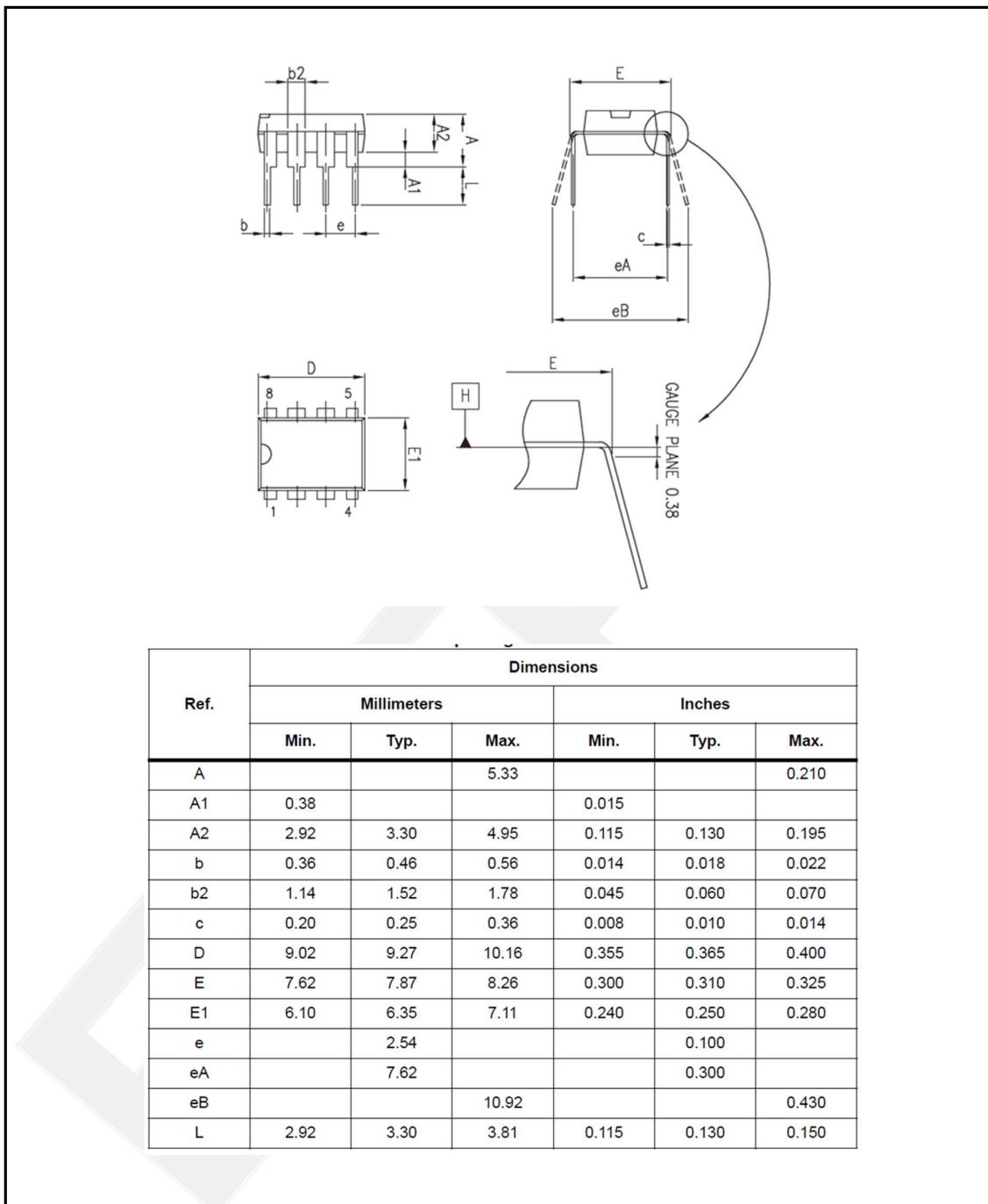


Figure 20 DFN10 Mechanical Data and Package Dimensions

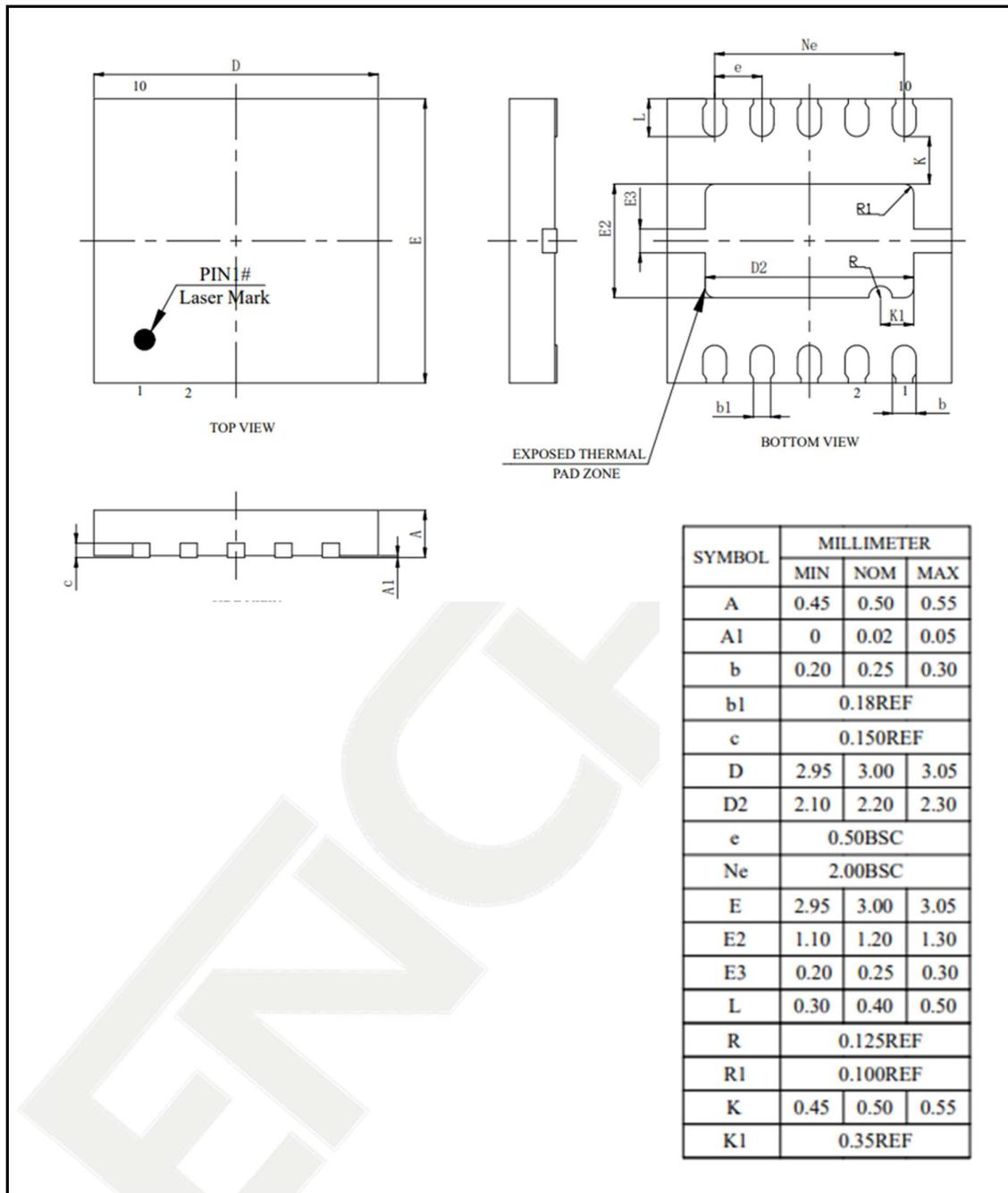


Figure 21 SSOP10 Mechanical Data and Package Dimensions

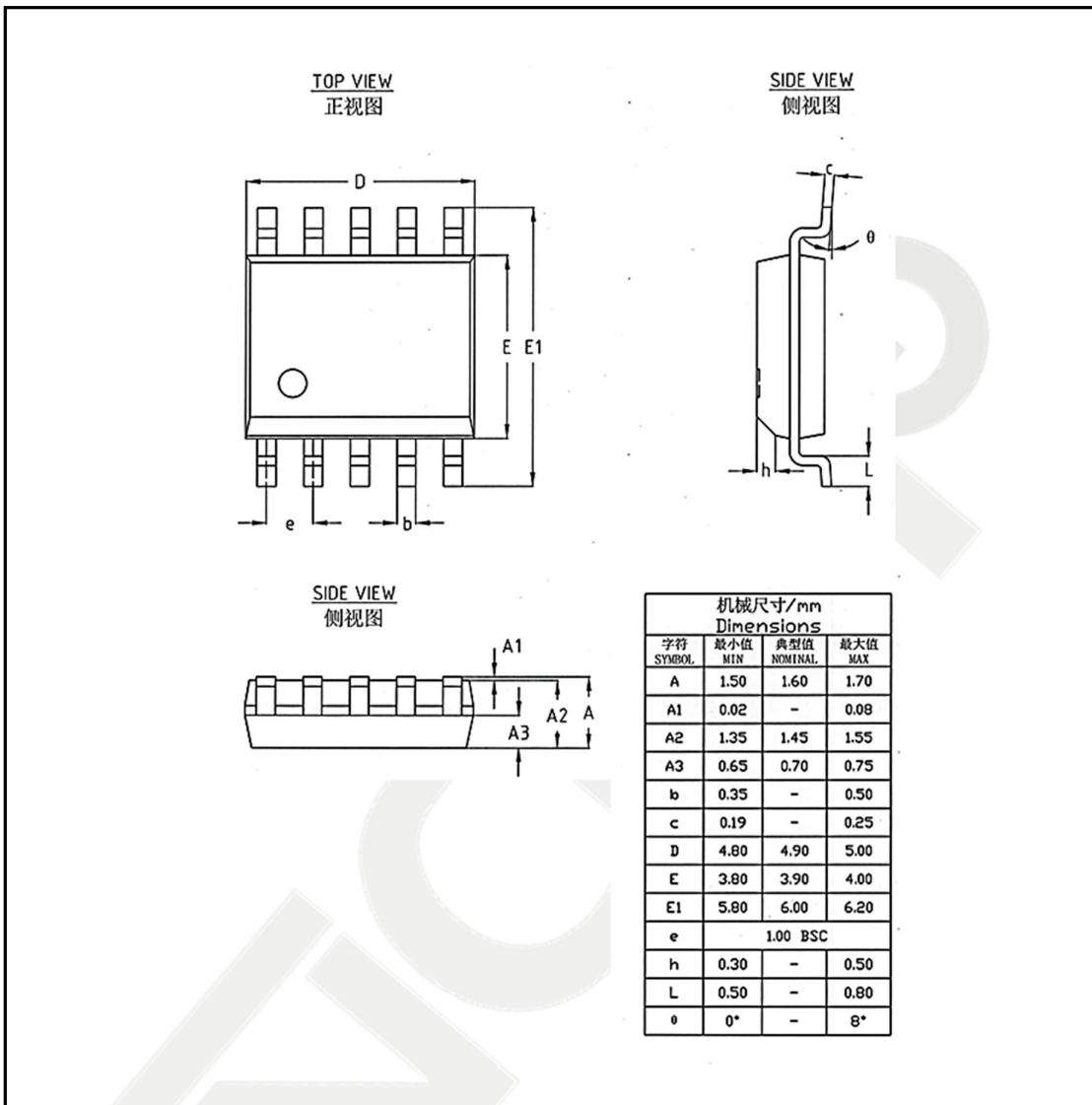


Figure 22 QFN14 Mechanical Data and Package Dimensions

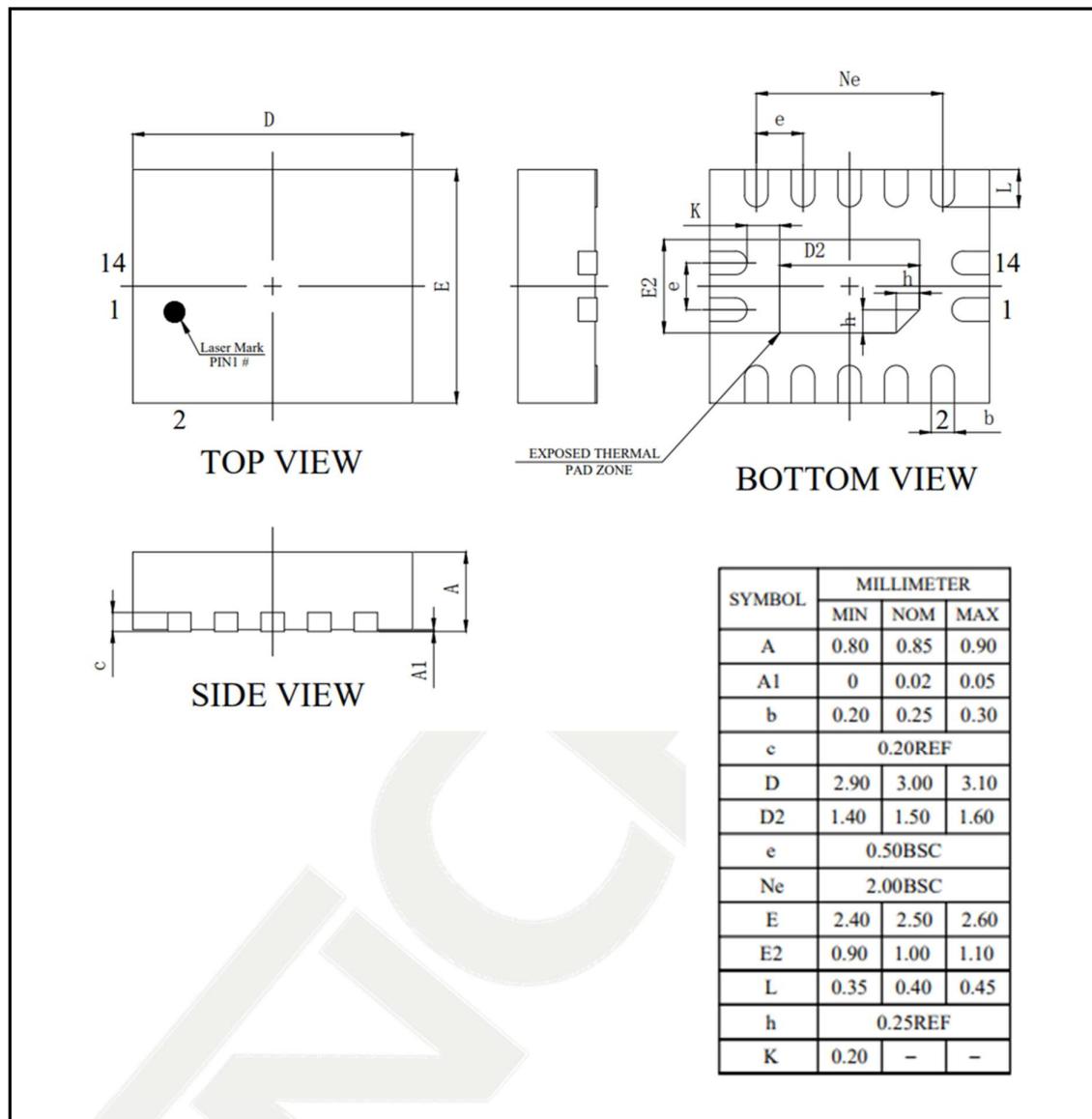


Figure 23 TSSOP14 Mechanical Data and Package Dimensions

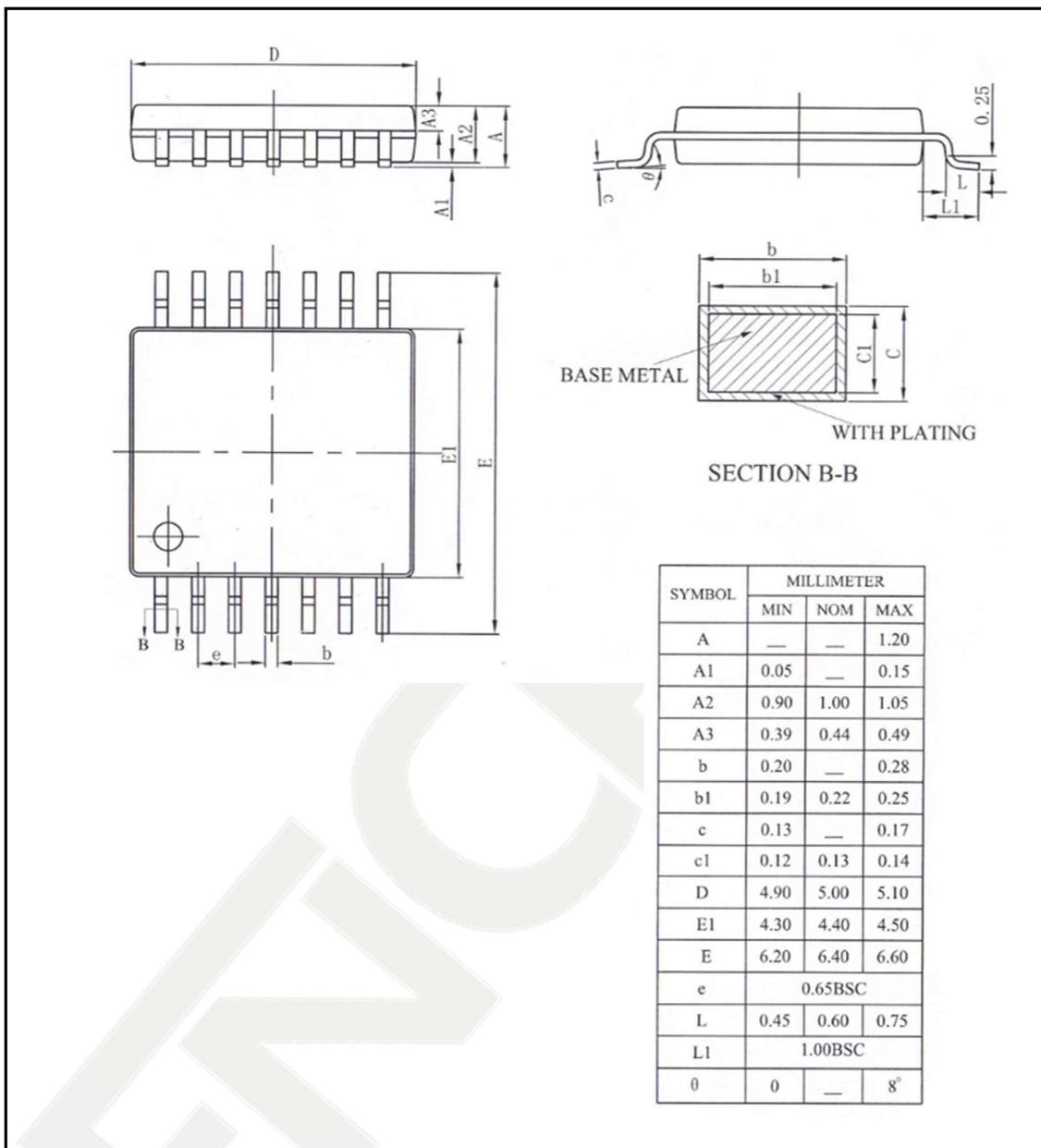


Figure 24 SOP14 Mechanical Data and Package Dimensions

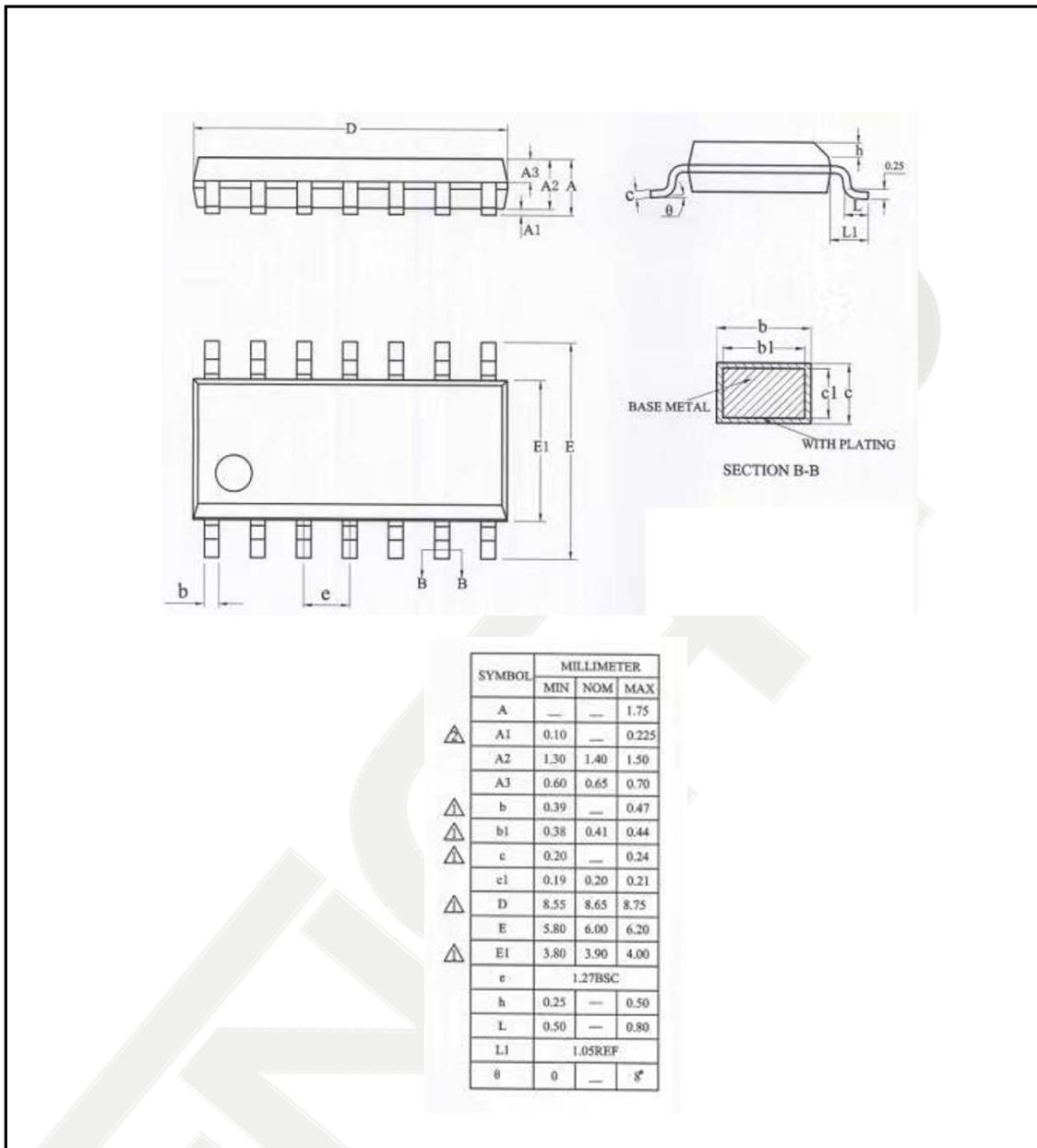


Figure 25 QFN16 Mechanical Data and Package Dimensions

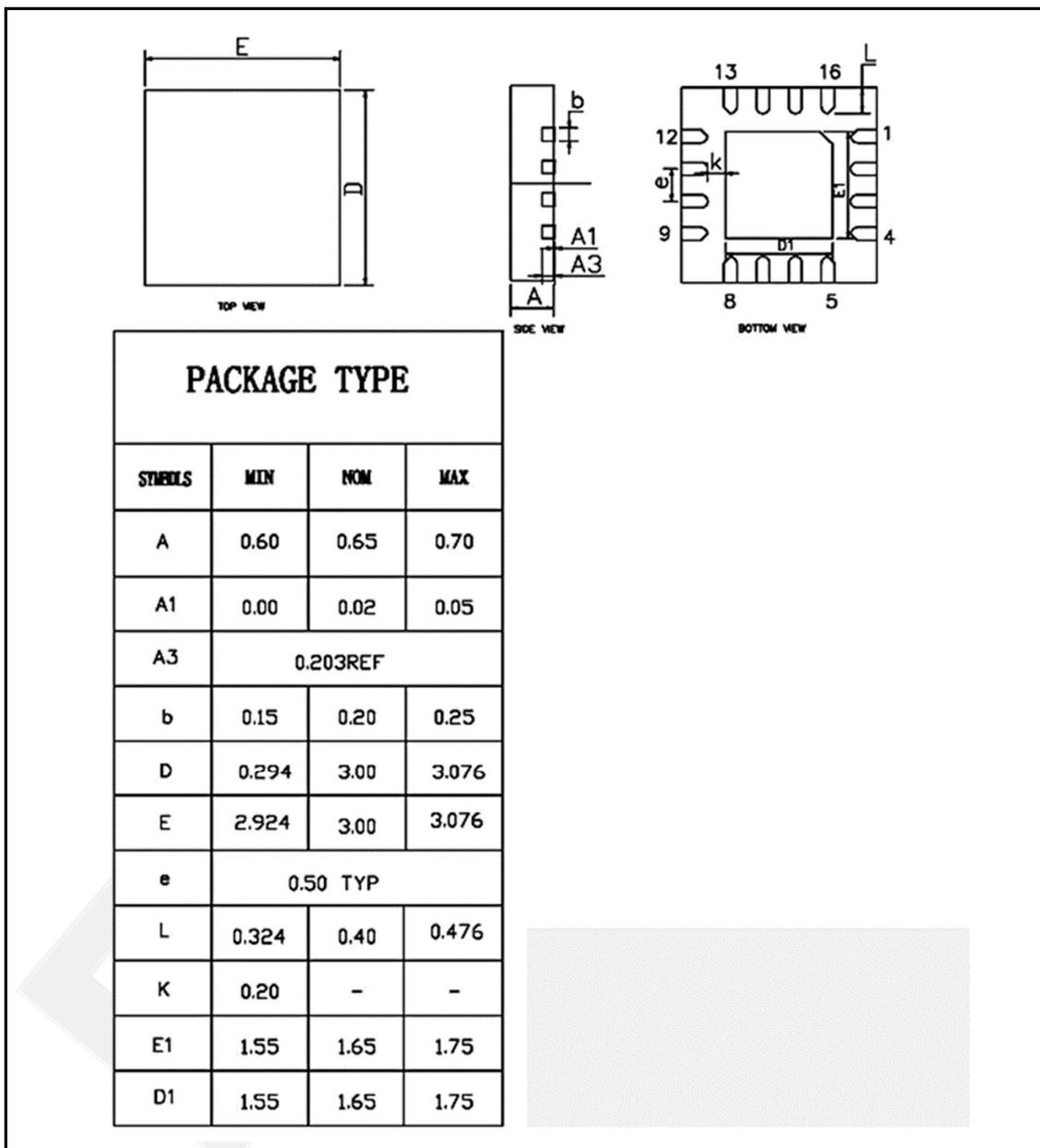
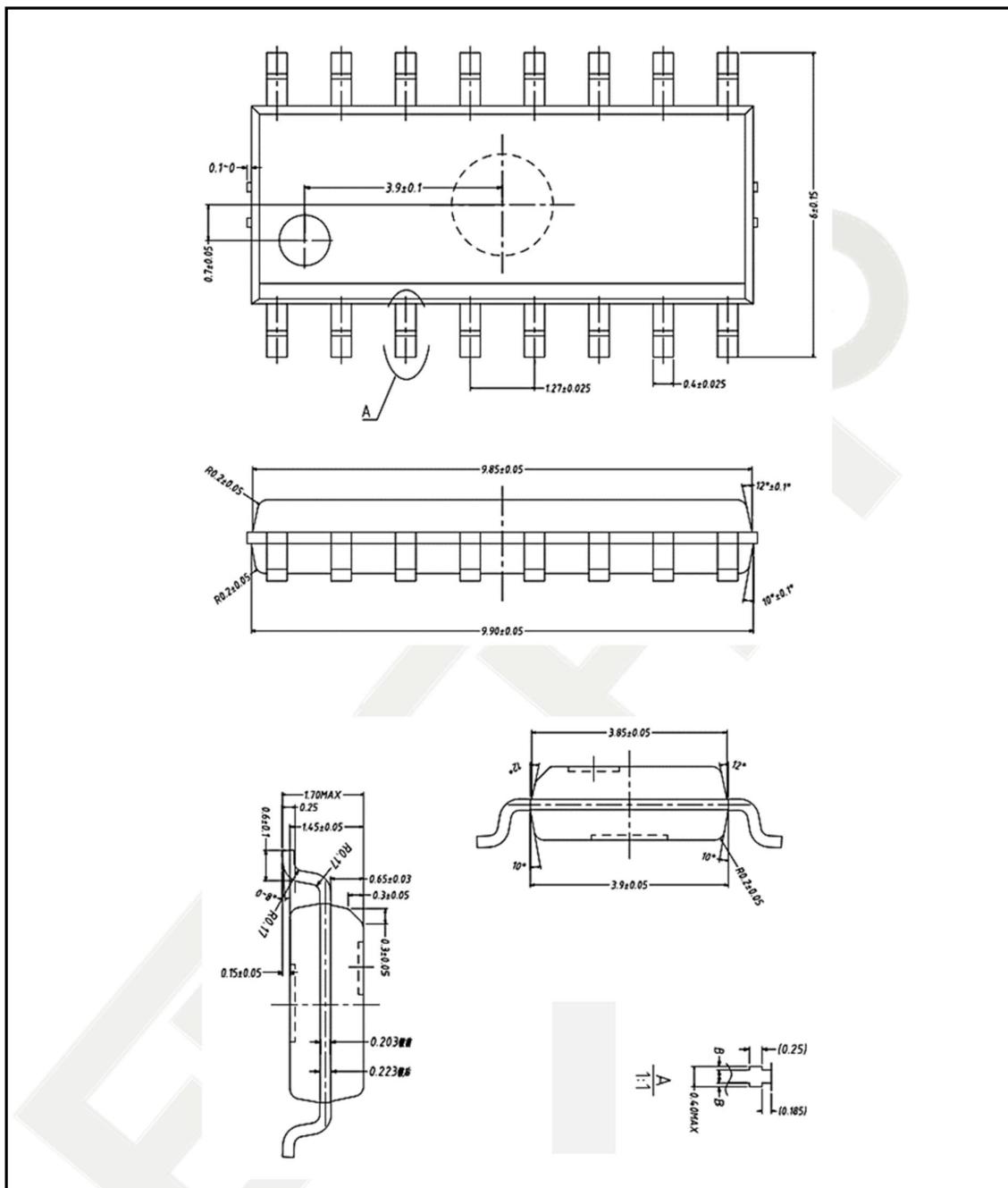


Figure 26 SOP16 Mechanical Data and Package Dimensions



5.2 Marking Information

Figure 27 eSOP8 Marking Information

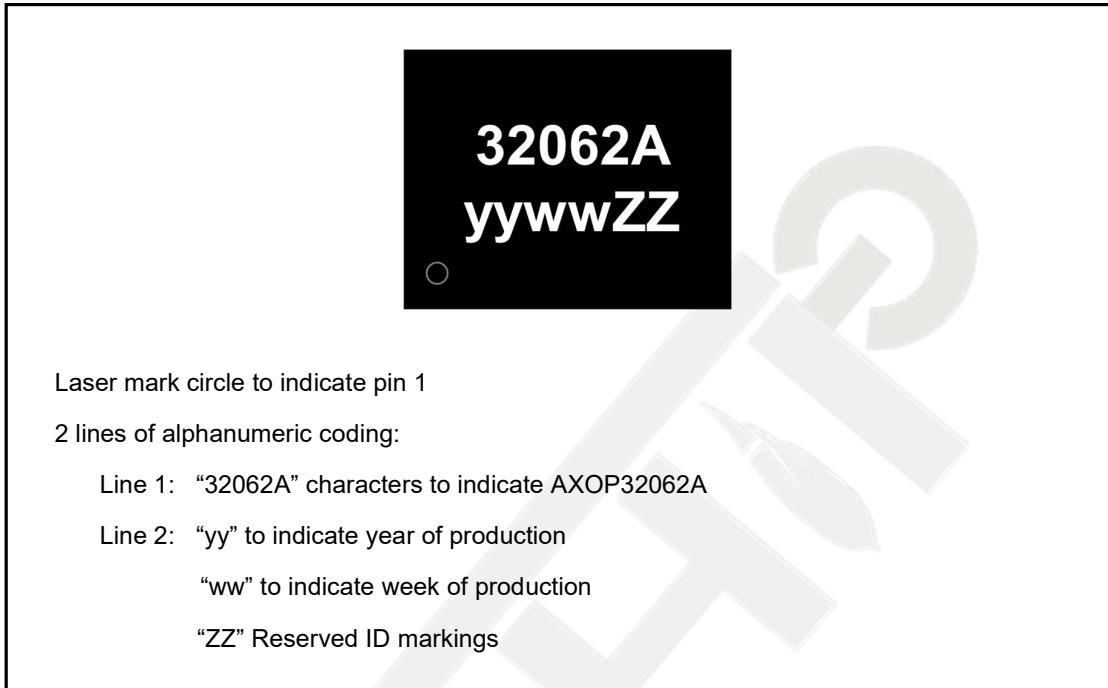


Figure 28 DFN8 Marking Information

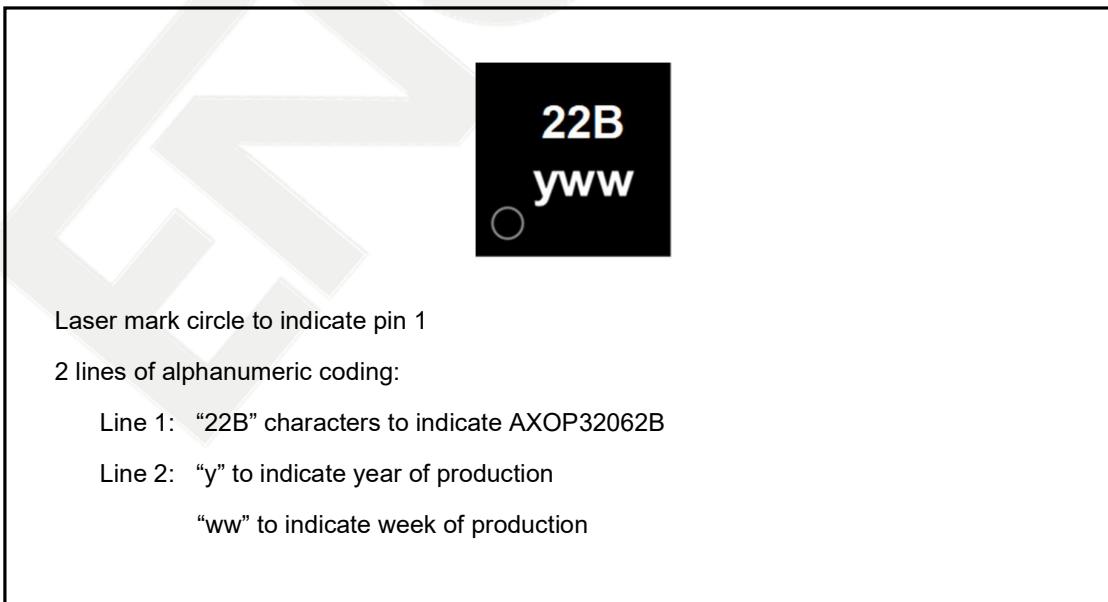


Figure 29 SOP8 Marking Information

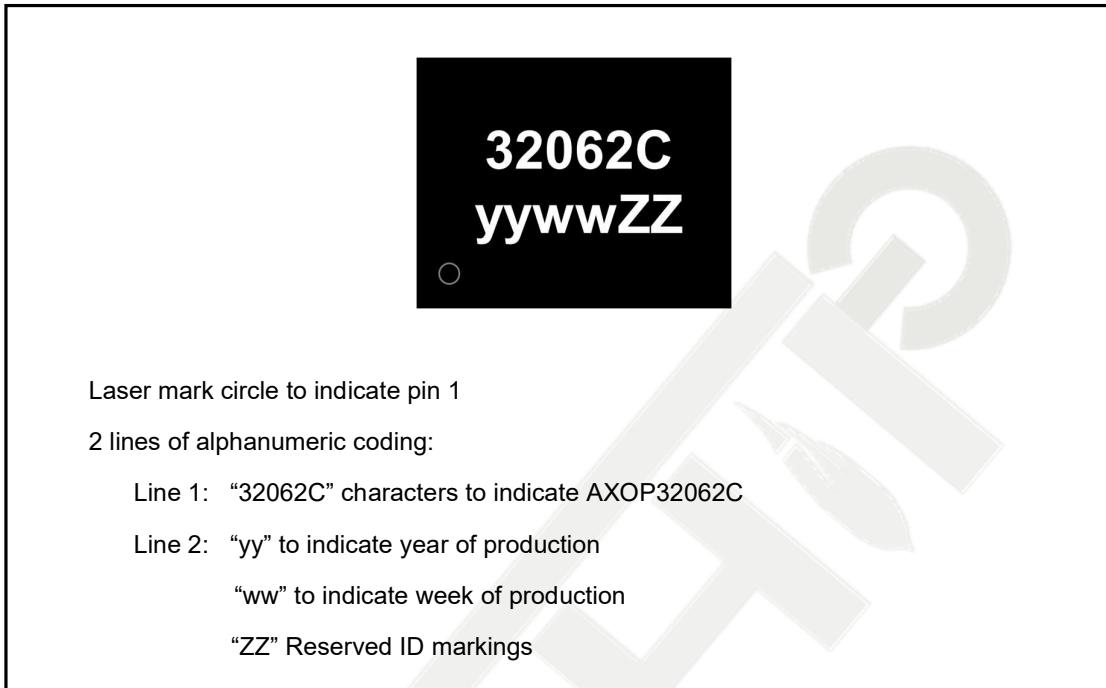


Figure 30 SOT23-8L Marking Information

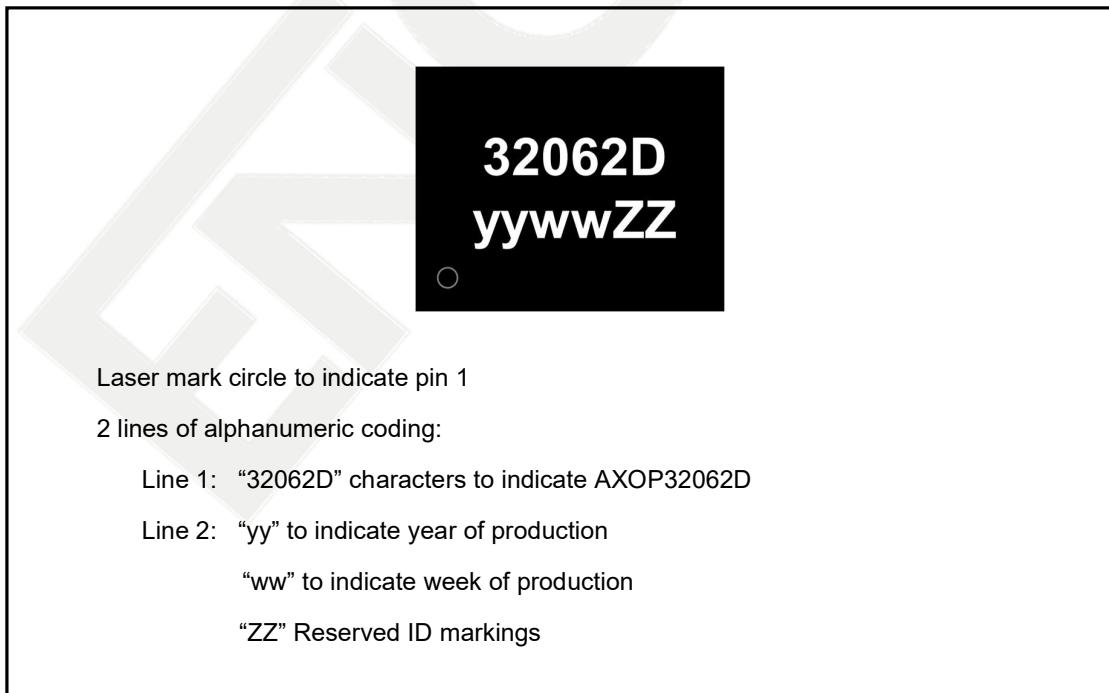


Figure 31 DIP8 Marking Information

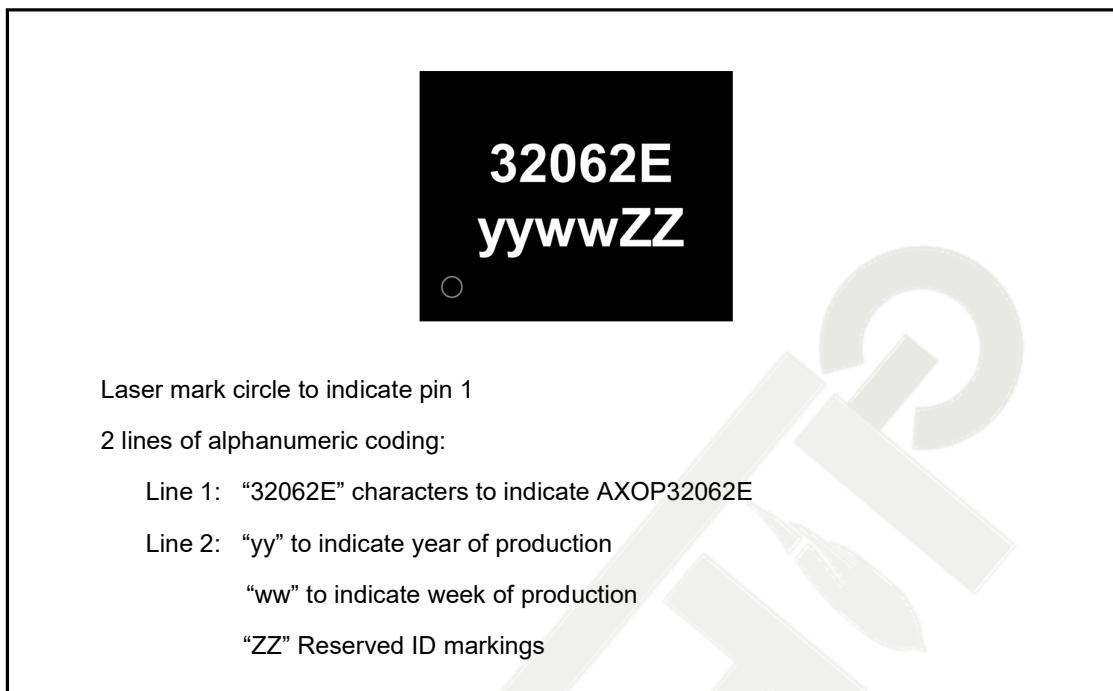


Figure 32 DFN10 Marking Information



Figure 33 SSOP10 Marking Information

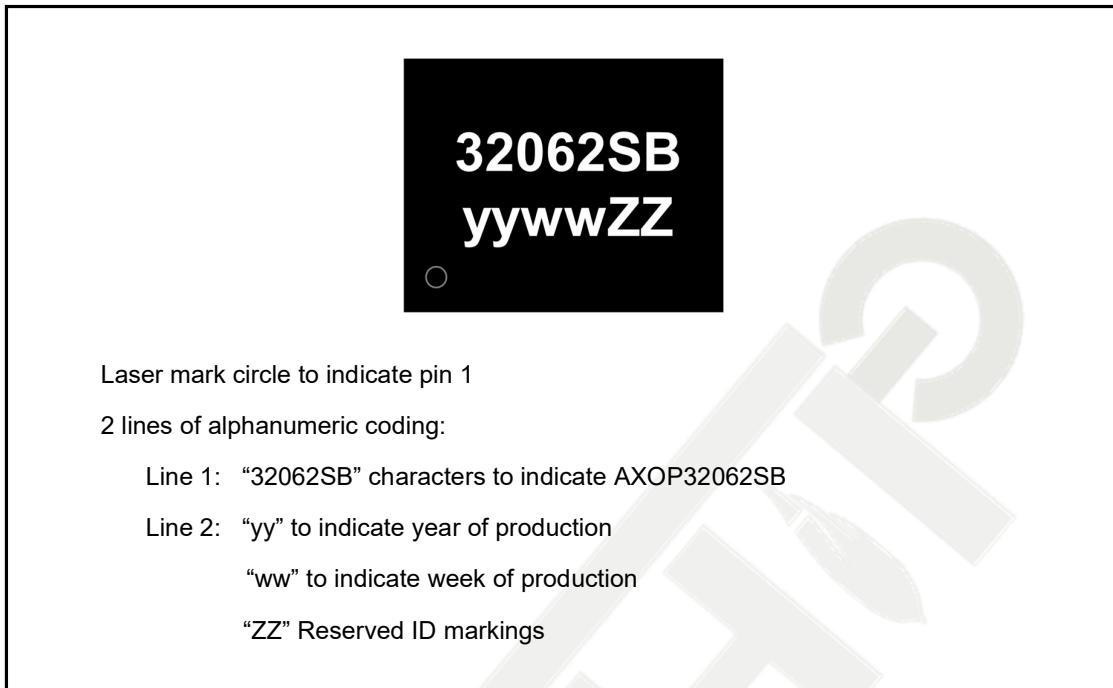


Figure 34 QFN14 Marking Information

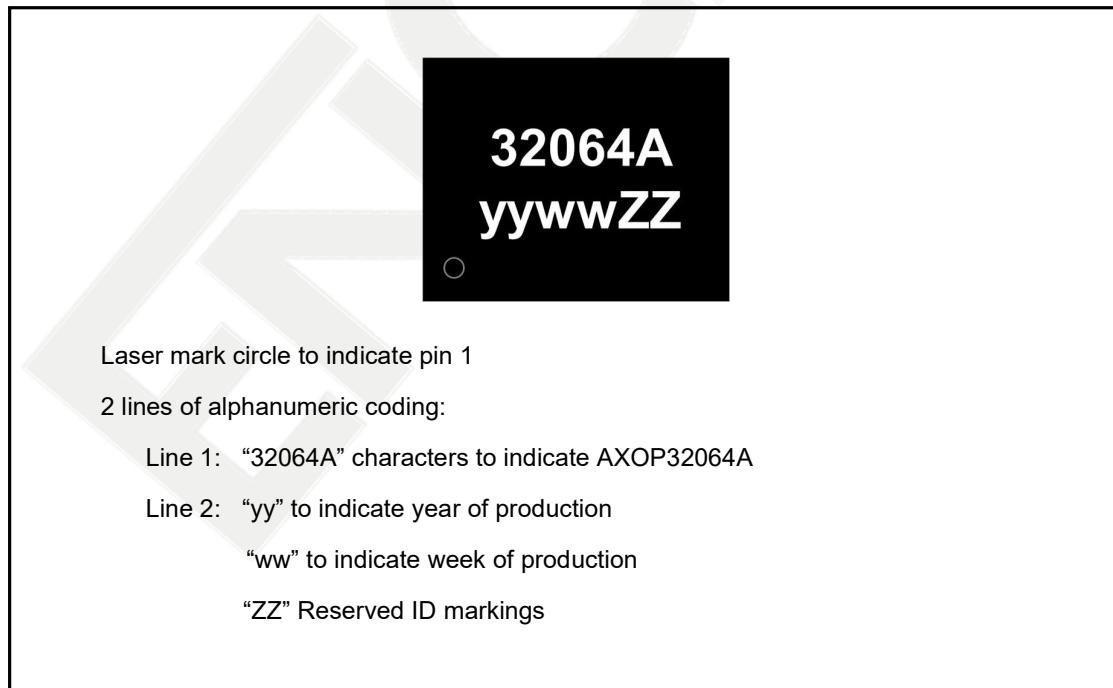


Figure 35 TSSOP14 Marking Information

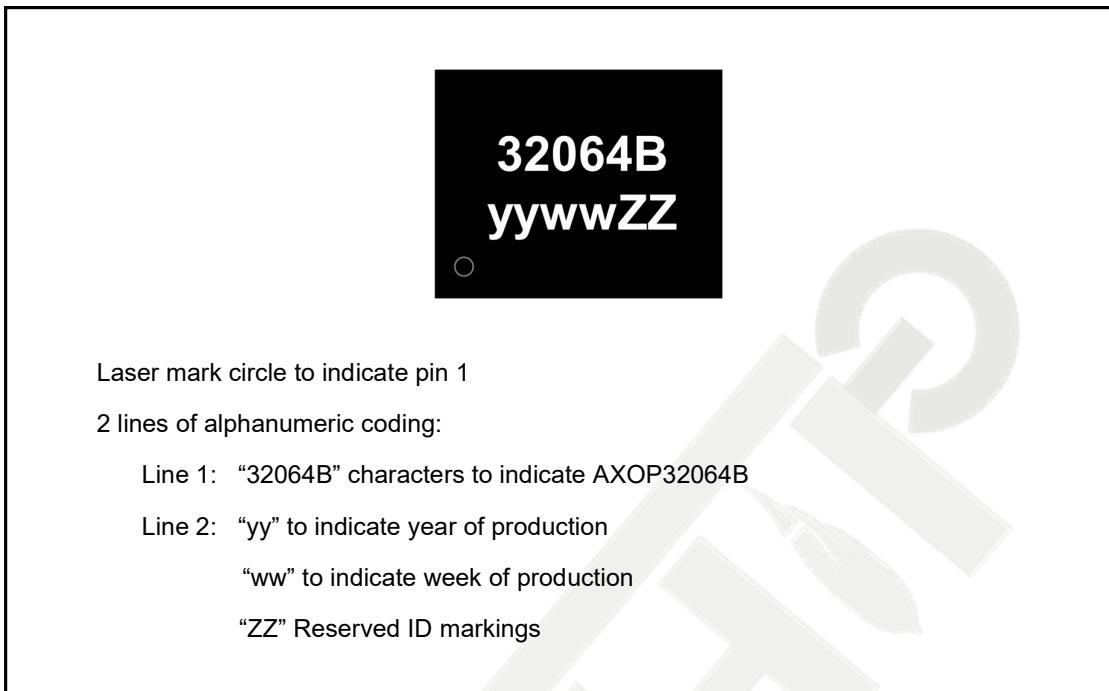


Figure 36 SOP14 Marking Information

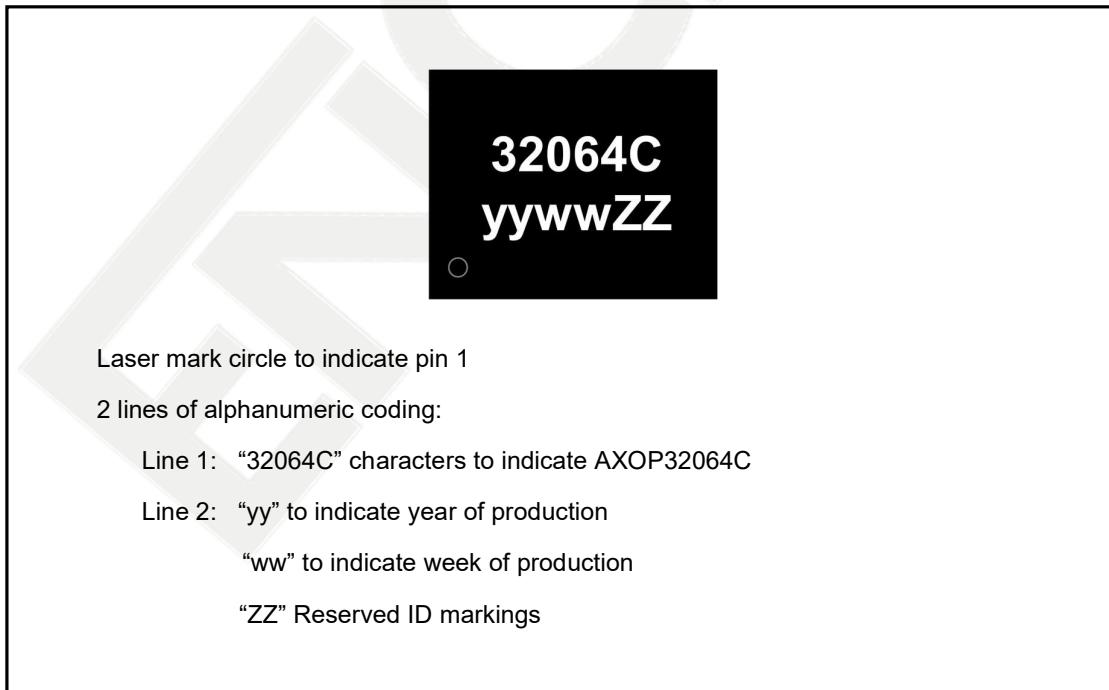


Figure 37 QFN16 Marking Information

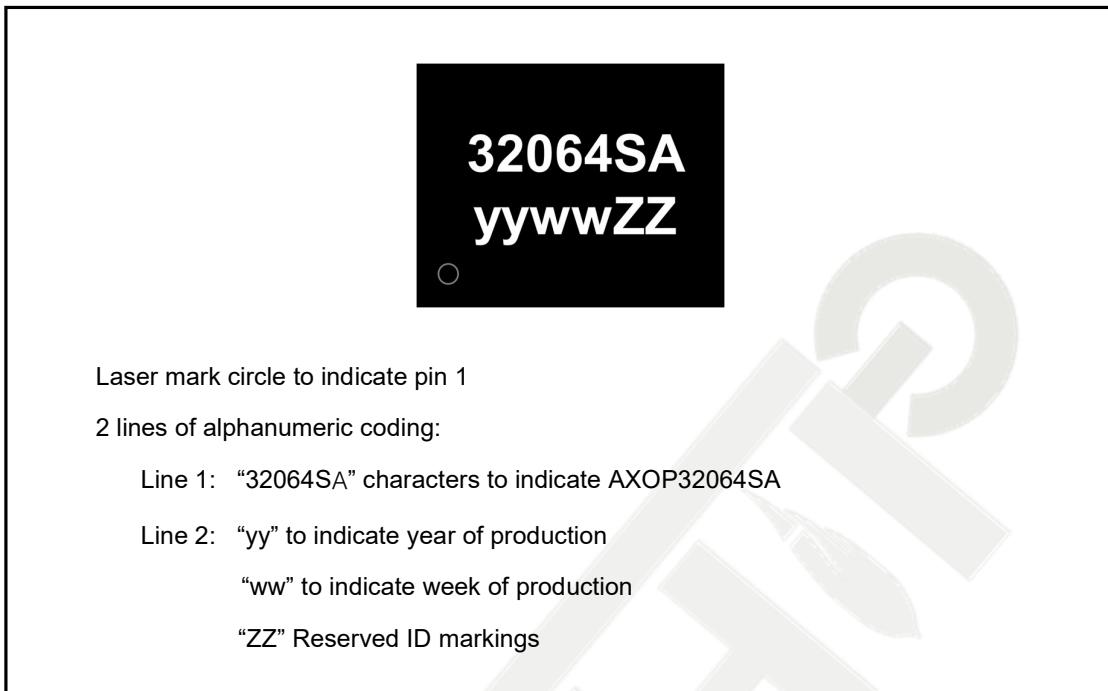
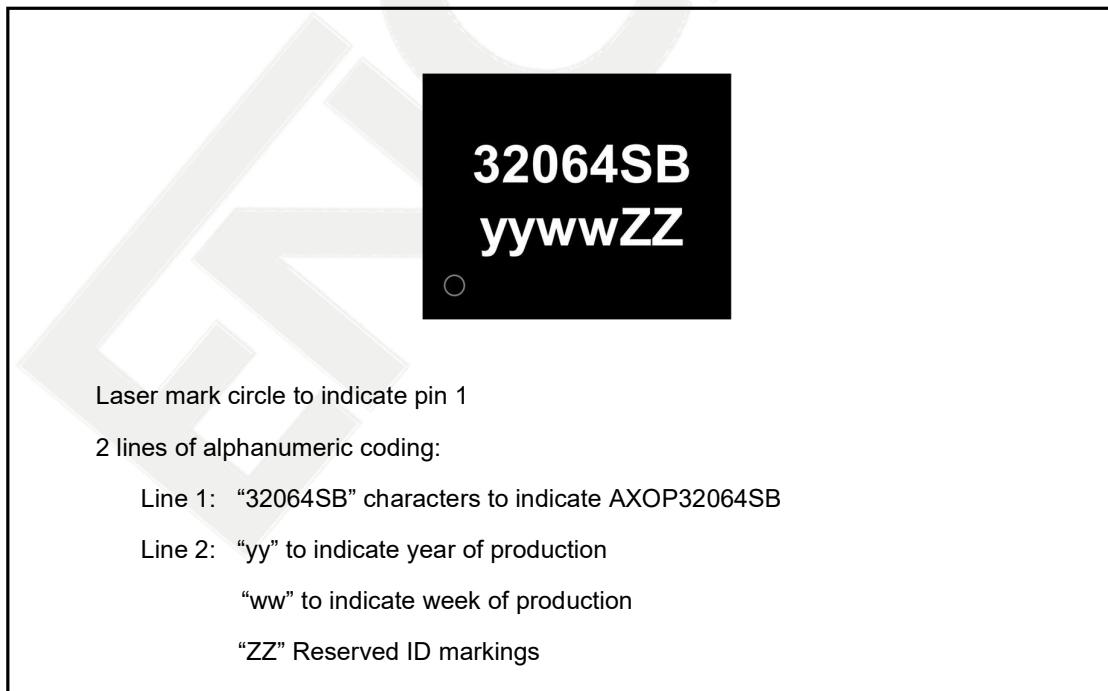
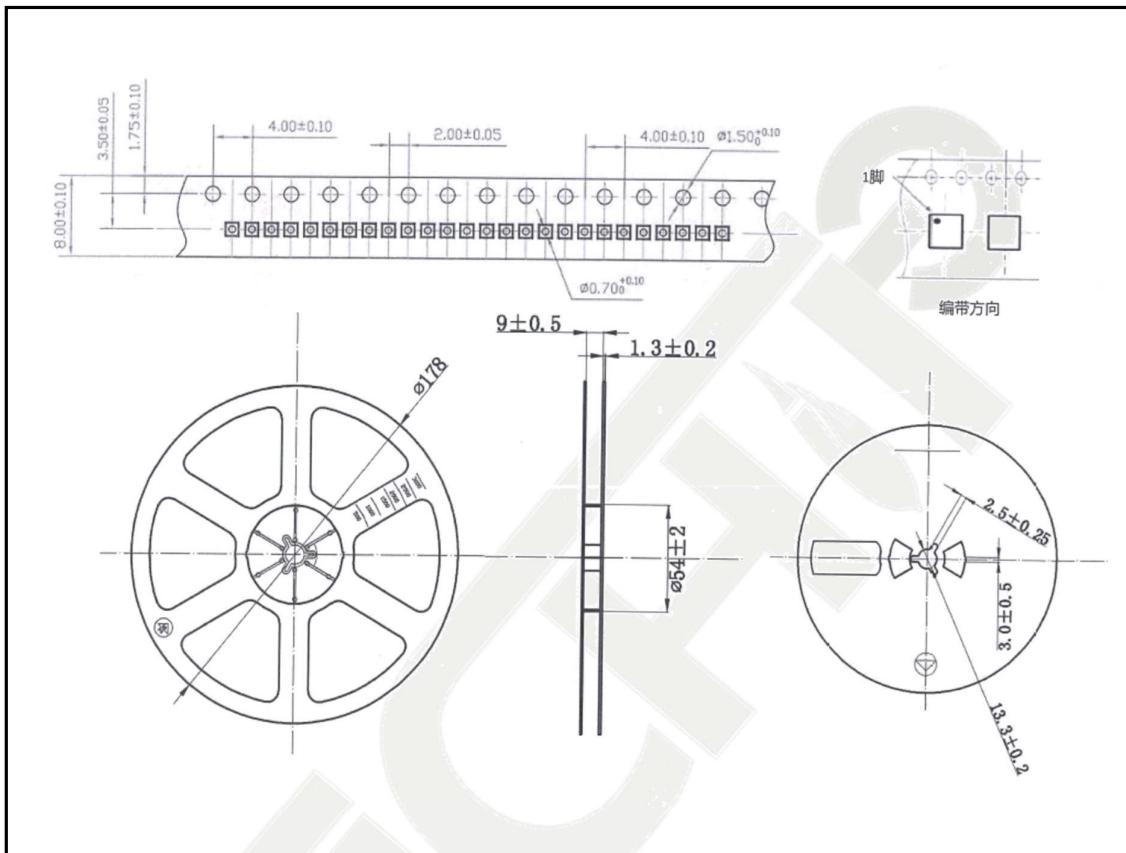


Figure 38 SOP16 Marking Information



6 Packing Information

Figure 39 Reel Packing Information



7 Revision History

Table 6 Document Revision History

Date	Version	Description
May 2023	1.00	V1.00 version.