AXPM415zxxyy

150mA / 500mA, Low VIN, Low VOUT Ultra-low Dropout Dual NMOS Regulator

Datasheet — June 2020

Description

AXPM415xxyy is a high accuracy, low quiescent current and ultra-low dropout dual regulator (LDO) that can source 150mA and 500mA respectively. Their dedicated NMOS pass transistor is biased by a common VBIAS pin allowing for ultra-low dropout performance at very low input voltages.

This enables increased efficiency and together with its low quiescent current, AXPM415xxyy is ideal for low power battery-operated, power-sensitive applications. Short circuit current foldback and thermal protection are included. It can be stabilized with a small capacitor at the output, saving on space overheads.

An independent enable logic control function puts corresponding LDO in shutdown mode, enabling a total current consumption of less than 0.1µA. Device options allows for active pull down at the output for discharge when disable.

Features

- Input voltage range: 0.8V to 5.5V
- Low quiescent current 25µA (typ) at no load
- Ultra-low dropout 65mV (typ) at 150 mA (LDO 1), 75mV (typ) at 500 mA (LDO 2)
- Available in 8 fixed-output voltages: 0.8V, 1.0V, 1.2V, 1.5V, 1.8V, 2.2V, 2.5V, 3.3V
- ±1% VOUT accuracy over Temperature
- High PSRR: 60dB at 1kHz
- Short circuit current limit with foldback
- Thermal shutdown

Applications

- Camera supply
- Mobile phones
- Tablets
- Battery-powered systems

Table 1 Device Summary

Order code	
AXPM415xxyy	xx (150mA LDO): 08=0.8V, 10=1.0V, 12=1.2V, 15=1.5V, 18=1.8V, 22=2.2V, 25=2.5V, 33=3.3V. yy (500mA LDO): 08=0.8V, 10=1.0V, 12=1.2V, 15=1.5V, 18=1.8V, 22=2.2V, 25=2.5V, 33=3.3V. Z A = 150mA + 150mA B = 150mA + 300mA C = = 150mA + 500mA

DFN8 epad
(3.0 x 3.0 x 0.75)

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1 Block Diagram and Application Circuit

Figure 1 Block Diagram (only 1 LDO indicated)

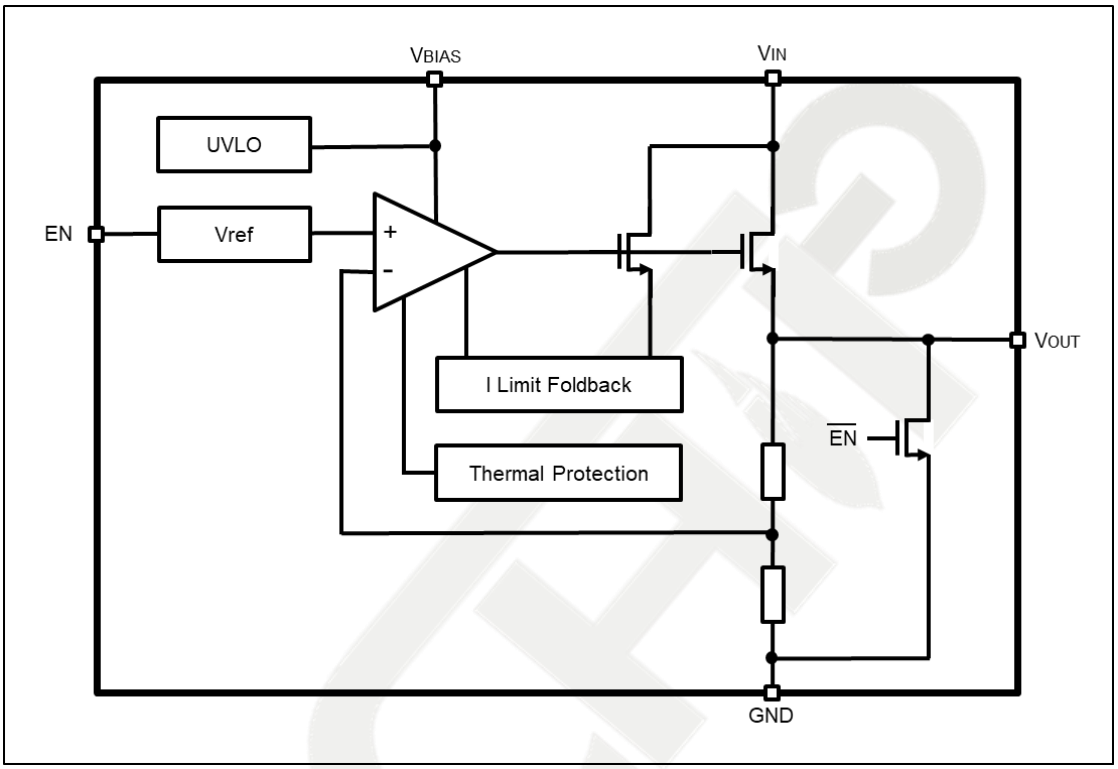
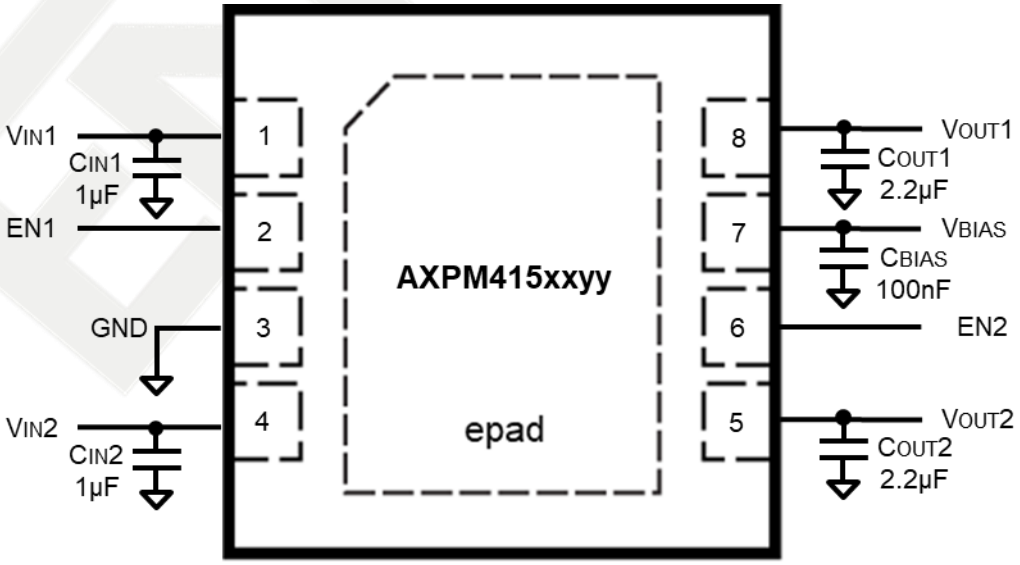


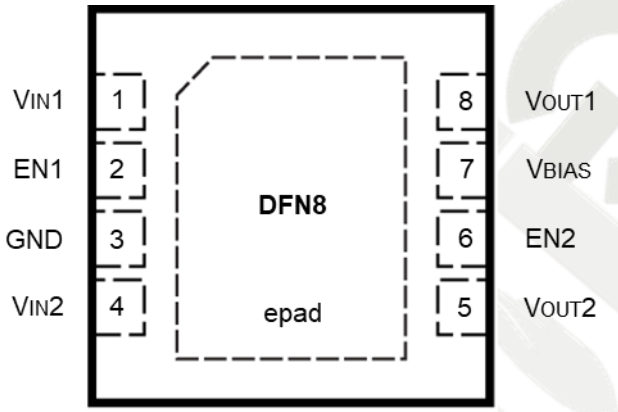
Figure 2 Application Circuit



2 Pin Description

2.1 Pin Names

Figure 3 Pin Connection



2.2 Pin Functions

Table 2 Pin Functions

Pin number	Pin name	Description
1	VIN1	Input supply voltage for LDO 1 (150mA)
2	EN1	Enable pin logic input for LDO 1: low=shutdown, high=active.
3	GND	Ground
4	VIN2	Input supply voltage for LDO 2 (500mA)
5	VOUT2	Output voltage for LDO 2 (500mA)
6	EN2	Enable pin logic input for LDO 2: low=shutdown, high=active.
7	VBIAS	Bias supply input
8	VOUT1	Output voltage for LDO 1 (150mA)
epad		Ground

3 Electrical Specifications

3.1 Absolute Maximum Ratings

Table 3 Absolute Maximum Ratings

Symbol	Parameter	Value	Unit
$V_{IN}1$, $V_{IN}2$	Input voltage	-0.3 to +7	V
V_{BIAS}	Input voltage (for driver)	-0.3 to +7	V
$V_{OUT}1$, $V_{OUT}2$	Output voltage	-0.3 to V_{IN}+0.3	V
$V_{EN}1$, $V_{EN}2$	Enable input voltage	-0.3 to +7	V
$I_{OUT}1$, $I_{OUT}2$	Output current	Internally limited	mA
PD	Power dissipation	Internally limited	mW
Tj	Junction temperature	+150	°C
Tstg	Storage temperature range	-55 to +150	°C

Note: Absolute maximum ratings are those values beyond which damage to the device may occur. The functional operation at or over these absolute maximum ratings is not assured.

3.2 Thermal Data

Table 4 Thermal Data

Symbol	Parameter	Value	Unit
Rth j-amb	Thermal resistance junction-to-case	5	°C/W
Rth j-case	Thermal resistance junction-to-ambient	43	°C/W

3.3 ESD and Latch Up

Table 5 ESD and Latch Up

Symbol	Parameter		Value	Unit
All pins	Electronics Static Discharge protection voltage	HBM	±2,000	V
		CDM	±500	V
All pins	Latch Up JESD78, Class A		≥ 100	mA

3.4 Electrical Characteristics

V_{IN} refers to $V_{IN}1$ or $V_{IN}2$. V_{OUT} refers to $V_{OUT}1$ or $V_{OUT}2$. V_{EN} refers to $V_{EN}1$ or $V_{EN}2$. V_{BIAS} = 2.7V or V_{OUT} + 1.6V (whichever is greater); V_{IN} = V_{OUT} + 0.3V; I_{OUT} = 1mA; C_{IN} = 1µF, C_{OUT} = 2.2µF; V_{EN} = 1V; typical values are at Tamb = 25°C; min/max values are at -40°C ≤ Tamb ≤ 85°C, unless otherwise specified.

Table 6 Electrical Characteristics

Symbol	Parameter	Test Conditions	Min	Typ	Max	Unit
V_{IN}	Operating input voltage		V_{OUT} + V_{DROP}		5.5	V
V_{BIAS}	Operating bias voltage	$V_{OUT}1$ and $V_{OUT}2$ ≤ 1V	2.4		5.5	V
		$V_{OUT}1$ or $V_{OUT}2$ > 1V; V_{OUT} is higher of $V_{OUT}1$ or $V_{OUT}2$	V_{OUT} + 1.4		5.5	V
T_{OP}	Operating temperature		-40		+85	°C
V_{UVLO}	BIAS under-voltage lockout	V_{BIAS} rising		1.6		V
		Hysteresis		0.2		
LDO 1 (150mA)						
$V_{OUT}1$	Output voltage accuracy		-0.5		+0.5	%
		$V_{OUT}1$ (nom) + 0.3V ≤ $V_{IN}1$ ≤ $V_{OUT}1$ (nom) + 1V; 2.7V or $V_{OUT}1$ (nom) + 1.6V (whichever is greater) ≤ V_{BIAS} ≤ 5.5V; $I_{OUT}1$ = 1mA to 150mA -40°C ≤ Tamb ≤ 85°C	-1.5		+1.5	%
$\Delta V_{OUT}1$-IN	$V_{IN}1$ line regulation (1)	$V_{OUT}1$ (nom) + 0.3V ≤ $V_{IN}1$ ≤ 5V; $I_{OUT}1$ = 1mA		0.02	0.1	%/V
$\Delta V_{OUT}1$-BIAS	V_{BIAS} line regulation (1)	2.7V or $V_{OUT}1$ (nom) + 1.6V (whichever is greater) ≤ V_{BIAS} ≤ 5.5V; $I_{OUT}1$ = 1mA		0.01	0.1	%/V
$\Delta V_{OUT}1$	Static load regulation	$I_{OUT}1$ = 1mA to 150mA		1.5		mV
V_{DROP}	Dropout voltage	$I_{OUT}1$ = 50mA; $V_{OUT}1$ = 97% of $V_{OUT}1$ (nom)		22	75	mV
		$I_{OUT}1$ = 150mA; $V_{OUT}1$ = 97% of $V_{OUT}1$ (nom)		65	250	
$V_{DROP}1$-BIAS	Dropout voltage	V_{BIAS} = $V_{IN}1$; $I_{OUT}1$ = 150mA		0.9	1.5	V
Vn1	Output noise voltage	$V_{OUT}1$ (nom) = 1.05V; $V_{IN}1$ = 1.5V 10Hz to 100kHz; $I_{OUT}1$ = 1mA		38		µV rms
$SVR_{IN}1$	$V_{IN}1$ supply voltage rejection	$V_{IN}1$ = $V_{OUT}1$ (nom) + 0.5V ± V_{RIPPLE}; V_{RIPPLE} = 0.2V, 1kHz;		75		dB

		$I_{OUT}1$ = 50mA; V_{BIAS} = 2.7V or $V_{OUT}1$ + 1.6V (whichever is greater)				
SVR_{BIAS}	V_{BIAS} supply voltage rejection	V_{BIAS} = 2.9V or $V_{OUT}1$ + 1.8V (whichever is greater) ± V_{RIPPLE}; V_{RIPPLE} = 0.2V, 1kHz; $I_{OUT}1$ = 50mA; $V_{IN}1$ = $V_{OUT}1$ (nom) + 0.5V		76		dB
I_{BIAS}	V_{BIAS} operating current	$I_{OUT}1$ = 0; V_{BIAS} = 2.7V		20	40	µA
IStby-BIAS	V_{BIAS} standby current	V_{BIAS} input current in OFF MODE: both $V_{EN}1$ = GND		0.03	1	µA
IStby-IN1	$V_{IN}1$ standby current	$V_{IN}1$ input current in OFF MODE: $V_{EN}1$ = GND		0.03	1	µA
$I_{LIM}1$	Output current limit	$V_{OUT}1$ = 0.9 x $V_{OUT}1$ (nom)	170	200	230	mA
$I_{SC}1$	Short circuit current	$V_{OUT}1$ = 0 (foldback protection)		50	150	mA
LDO 2 (500mA)						
$V_{OUT}2$	Output voltage accuracy		-0.5		+0.5	%
		$V_{OUT}2$ (nom) + 0.3V ≤ $V_{IN}2$ ≤ $V_{OUT}2$ (nom) + 1V; 2.7V or $V_{OUT}2$ (nom) + 1.6V (whichever is greater) ≤ V_{BIAS} ≤ 5.5V; $I_{OUT}2$ = 1mA to 500mA -40°C ≤ Tamb ≤ 85°C	-1.5		+1.5	%
$\Delta V_{OUT}2$-IN	$V_{IN}2$ line regulation (1)	$V_{OUT}2$ (nom) + 0.3V ≤ $V_{IN}2$ ≤ 5V; $I_{OUT}2$ = 1mA		0.02	0.1	%/V
$\Delta V_{OUT}2$-BIAS	V_{BIAS} line regulation (1)	2.7V or $V_{OUT}2$ (nom) + 1.6V (whichever is greater) ≤ V_{BIAS} ≤ 5.5V; $I_{OUT}2$ = 1mA		0.01	0.1	%/V
$\Delta V_{OUT}2$	Static load regulation	$I_{OUT}2$ = 1mA to 150mA		1.5		mV
$V_{DROP}2$	Dropout voltage	$I_{OUT}2$ = 150mA; $V_{OUT}2$ = 97% of $V_{OUT}2$ (nom)		25	75	mV
		$I_{OUT}2$ = 500mA; $V_{OUT}2$ = 97% of $V_{OUT}2$ (nom)		80	250	
$V_{DROP}2$-BIAS	Dropout voltage	V_{BIAS} = $V_{IN}2$; $I_{OUT}2$ = 500mA		0.9	1.5	V
Vn2	Output noise voltage	$V_{OUT}2$ (nom) = 1.05V; $V_{IN}2$ = 1.5V 10Hz to 100kHz;		38		µV rms

		$I_{OUT}2$ = 1mA				
$SVR_{IN}2$	$V_{IN}2$ supply voltage rejection	$V_{IN}2 = V_{OUT}2$ (nom) + 0.5V ± V_{RIPPLE}; V_{RIPPLE} = 0.2V, 1kHz; $I_{OUT}2$ = 150mA; V_{BIAS} = 2.7V or $V_{OUT}2$ + 1.6V (whichever is greater)		75		dB
SVR_{BIAS}	V_{BIAS} supply voltage rejection	V_{BIAS} = 2.9V or $V_{OUT}2$ + 1.8V (whichever is greater) ± V_{RIPPLE}; V_{RIPPLE} = 0.2V, 1kHz; $I_{OUT}2$ = 150mA; $V_{IN}2 = V_{OUT}2$ (nom) + 0.5V		76		dB
I_{BIAS}	V_{BIAS} operating current	$I_{OUT}2$ = 0; V_{BIAS} = 2.7V		27	40	µA
IStby-BIAS	V_{BIAS} standby current	V_{BIAS} input current in OFF MODE: both $V_{EN}2$ = GND		0.03	1	µA
IStby-IN2	$V_{IN}2$ standby current	$V_{IN}2$ input current in OFF MODE: $V_{EN}2$ = GND		0.03	1	µA
$I_{LIM}2$	Output current limit	$V_{OUT}2$ = 0.9 x $V_{OUT}2$ (nom)	550	700	1,000	mA
$I_{SC}2$	Short circuit current	$V_{OUT}2$ = 0 (foldback protection)		365	500	mA
Others						
$V_{EN}1$, $V_{EN}2$	Enable logic low				0.4	V
	Enable logic high		0.9			
$I_{EN}1$, $I_{EN}2$	Enable input current	V_{EN} = 5.5V			400	nA
T_{ON} (2)	Turn on time	V_{OUT} (nom) = 1V		110		µs
T_{SD}	Thermal shutdown			160		°C
	Hysteresis			20		°C
C_{OUT}	Output capacitor		1	2.2	22	µF

(1) Not applicable for V_{OUT} (nom) ≥ 5V.
(2) Turn-on time is time measured between the enable input just exceeding V_{EN} high value and the output voltage just reaching 98% of its nominal value.

4 Functional Description

4.1 V_{BIAS} Voltage Requirement

V_{BIAS} is used for the driving of the NMOS pass channel. The pin must have a minimum voltage of 2.4V and 1.6V (typically) higher than the output for proper operation. In the event V_{IN} supply is meeting the bias requirement, V_{BIAS} can be connected directly to V_{IN}.

4.2 Output Discharge Function

A discharge mosfet is available at V_{OUT} for quick discharge of the output capacitor when device is disabled (EN = low). Optional devices are also available without this discharge mosfet function.

4.3 Short Circuit and Current Limitation

Short circuit current limit foldback protection is integrated. The load current is limited to I_{LIM} when V_{OUT} is equal to 90% of its nominal value. On further decreasing V_{OUT} due to low impedance short circuit, foldback circuit starts operating, limiting the current to I_{SC} when V_{OUT} = 0.

4.4 Thermal Protection

AXPM415xxyy is protected with thermal shutdown when the junction temperature reaches 160°C typical. It recovers upon cooling and reaching thermal hysteresis value.

4.5 Input and Output Capacitors

External capacitors are required to ensure the regulator control loop stability. For the input and outputs capacitors, a minimum of 1µF for C_{IN}, a minimum of 100nF for C_{BIAS} and a minimum of 1µF (with ESR 3 to 300mΩ) for C_{OUT} are required.

Good quality ceramic capacitors such as the X5R and the X7R are suggested. Further care in placing capacitors close to the pins with low impedance routing and with good return Analog ground minimization of noise pickup. Along with good capacitors having low variations across operation conditions, excellent performance can be achieved with AXPM415xxyy.

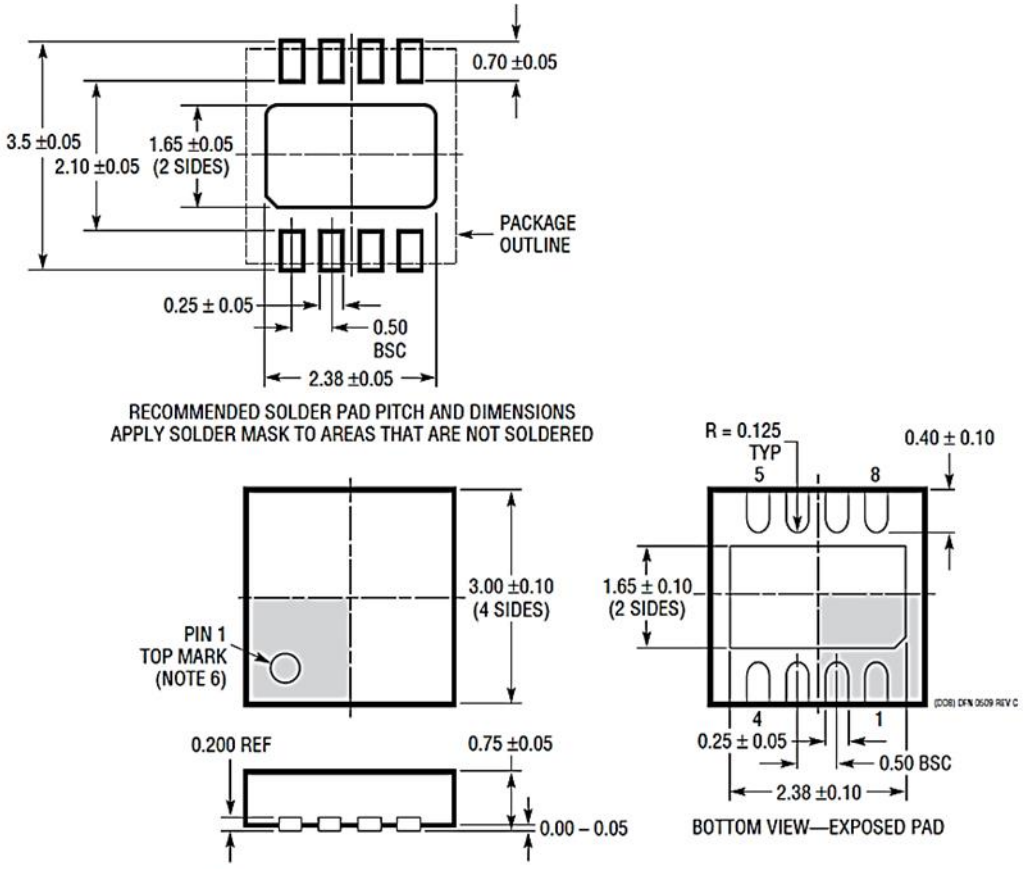
4.6 Under-voltage Lockout (UVLO)

An under-voltage lockout function for V_{BIAS} is included. On powering up, lockout is maintained till V_{BIAS} reaches 1.6V. A hysteresis of 0.2V is designed in to ensure clean entry and exit from the lockout.

4.7 Typical Performances

5 Package Information

Figure 4 DFN8 EPAD 3.0 x 3.0 x 0.75 Mechanical Data and Package Dimensions



NOTE:
1. DRAWING TO BE MADE A JEDEC PACKAGE OUTLINE M0-229 VARIATION OF (WEED-1)
2. DRAWING NOT TO SCALE
3. ALL DIMENSIONS ARE IN MILLIMETERS
4. DIMENSIONS OF EXPOSED PAD ON BOTTOM OF PACKAGE DO NOT INCLUDE MOLD FLASH. MOLD FLASH, IF PRESENT, SHALL NOT EXCEED 0.15mm ON ANY SIDE
5. EXPOSED PAD SHALL BE SOLDER PLATED
6. SHADED AREA IS ONLY A REFERENCE FOR PIN 1 LOCATION ON TOP AND BOTTOM OF PACKAGE

6 Revision History

Table 7 Document Revision History

Date	Version	Description
Jun 2020	1.00	First version.